威视锐 V3 Technology,.Ltd. | Make Radio Programmable

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YunSDR Y750Neo

Covering a full frequency band of 400MHz bandwidth below 8GHz,4x4 MIMO software defined radio

- Covering the frequency range of 1 MHz to 8 GHz
- Four channel real-time transmission and reception bandwidth of 400MHz
- 2x100G high-speed data transmission interface, standard PCIe 3.0 front card, additional massive FPGA logic resources provided
- Ready to use software toolkit, supporting RF acquisition, recording, and playback
- Rich secondary development API resources, cross platform support for MATLAB, Python, C #, C/C++, etc
- Integrated open-source GNU Radio development environment, capable of directly running open-source 4G and 5G protocol stacks



Real-time

Networkable

Open APIs

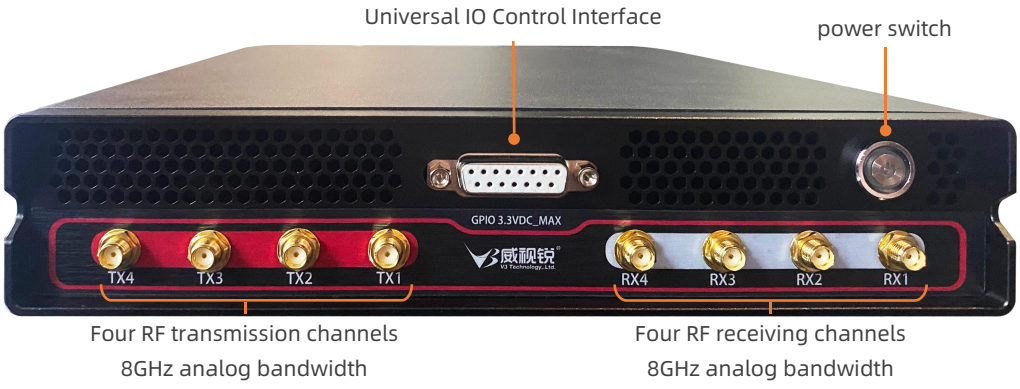
Easy integration

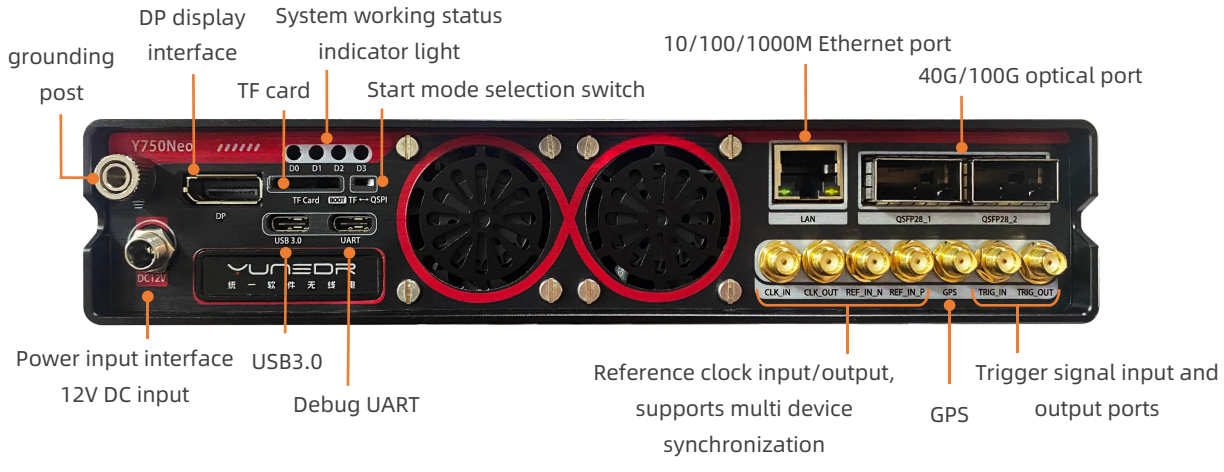
V3 technology (Beijing) LTD

Product description

YunSDR Y750Neo is the latest flagship model of the 7 series, targeting the emerging 7.2GHz frequency band of 5G and WiFi7. It adopts high-performance RF front-end and third-generation Xilinx Zynq UltraScale+RFSoC construction, meeting the verification and development of next-generation wireless communication standards. As a high-performance multi-channel software defined radio platform, the frequency range is from 1MHz to 8GHz, supporting four independent transmission and reception channels, with an instantaneous bandwidth of up to 400MHz. The sampling rate of high-speed ADC can reach up to 5GSPS with an accuracy of 14 bits, while the sampling rate of high-speed DAC can reach up to 9.85GSPS with an accuracy of 14 bits. The data transmission interface adopts 100G optical fiber, and real-time interaction with the upper computer is achieved through a PCIe3.0x16 programmable FPGA front-end card. In addition, the device provides standard control and debugging interfaces, including USB-JAG, 10/100/1000M Ethernet, TF card, USB3.0, etc. The start mode switch can flexibly configure various start modes, with 12V DC power supply.

Schematic diagram of the YunSDR Y750neo interface of V3





At present, the signal bandwidth of WiFi6 is 160MHz, WiFi7 will reach 320MHz, and the bandwidth of 5G millimeter wave and NTN standards can reach up to 400MHz. So, YunSDR Y750Neo not only meets the high bandwidth requirements of existing commercial protocols, but also supports future communication standards such as 6G millimeter wave and broadband satellite communication. For fields such as spectrum analysis and RF recording playback, the more comprehensive the information that can be observed simultaneously with 8GHz full frequency coverage, the more it can replace traditional high-end instruments or multiple devices.

Main features and interfaces:

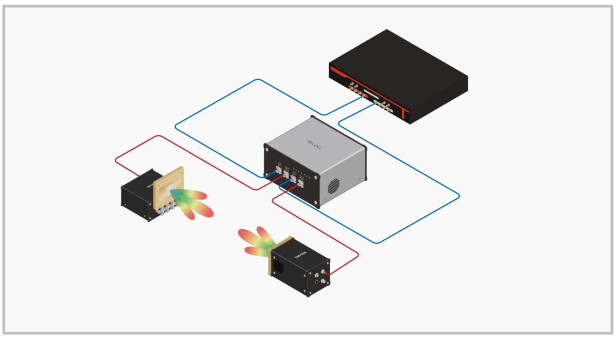
High performance, channel density, and high integration
Two development modes: standalone mode (embedded) or host mode (100G to PCIe streaming mode)
1 MHz to 8GHz frequency range (expandable to millimeter wave frequency band)
Real time bandwidth 400MHz mode
4-channel transmission, 4-channel reception
Xilinx Zynq-Ultrascale+ ZU47DR RFSoC
14 bit ADC, 14 bit DAC
IQ sampling clock 500MSP, supporting 983.04MSPS and 960MSPS simultaneously
Four core ARM Cortex-A53 processor, with a maximum clock speed of 1.2 GHz
Four core ARM Cortex-A5 MPCore processor, with a maximum clock speed of 400 MHz
2 x QSFP28 optical ports (supporting 40G/100G Aurora and custom protocols)
Provide PCIe fronthaul acceleration card, PCIe Gen3 x 16 interface, Xilinx Kintex Ultra Scale+KU15P FPGA, 2 QSFP28 optical ports
Gigabit Ethernet RJ45
Reference clock input/output
Trigger signal input/output
Built in GPSDO
FPGA GPIO interface
USB 3.0 Host/Device Interface
Type C USB port serial console, JTAG)

8GHz coverage for mainstream applications

The current wireless communication standard is basically within 6GHz, and the next generation of WiFi7 and 5G private networks will use the 7.125GHz frequency band. YunSDR Y750Neo provides a complete solution that supports 5G FR1 frequency band and some FR3 frequency bands (6GHz~8GHz). Through the matching up and down converters, it can support continuous frequency conversion from 24GHz to 44GHz, with a bandwidth of 400MHz mode. It also provides 4x4 and 8x8 phased array antennas, which meet the research requirements of 5G millimeter wave communication and beamforming, and also support the technological exploration of future 6G standards.



Millimeter wave antenna component of YunSDR Y750Neo



Building a complete millimeter wave prototype verification and testing platform based on YunSDR Y750Neo and its millimeter wave components

The number of channels can be expanded

RFSoC, as an innovative device for wireless communication, integrates embedded processors, data converters (ADC/DAC), and programmable FPGAs for the first time. A single chip can provide up to 32 transmit and receive channels (16T/16R). The YunSDR Y750Neo offers four transmit and four receive channels, while the Y790s in the same series can provide eight transmit and eight receive channels. The Matrix RF series MRF16 can provide 16 transmit and receive channels.

The YunSDR Y750Neo integrates four transmission channels and four reception channels into a compact half rack with a 1U height broadband, making it easier to transport for on-site testing and operation. Each channel is independent, which means that each channel can be tuned to different frequencies for frequency division multiplexing (FDD) applications or for simulating multiple signals simultaneously. The channel can also be synchronized through an internal constant temperature crystal oscillator (OCXO), and an internal GPS taming oscillator (GPSDO) is used for timestamps, providing a 10 MHz reference and pulses per second (PPS).

Rack mounted spliceable structure

Every two devices can be assembled into a standard 1U 19 inch chassis, and more chassis can be combined with more antennas.

Customized rack structure | Internal clock synchronization | Specialized calibration kit

For applications with higher channel counts, it is recommended to use MatrixRF series products with VPX architecture. MatrixRF is designed for Massive MIMO and array signal processing scenarios, providing an array based software defined radio platform with phase synchronization. It enables high bandwidth multi-channel configurable system combinations, supports channel numbers from 16x16 to 256x256, adapts to elastic bandwidths of 20KHz~2GHz, and meets scenarios such as 5G/6G system prototyping, channel simulation testing, and radar signal simulation.



High performance baseband and high-speed interface

With the increase in the number of channels and bandwidth, the massive amount of baseband data undoubtedly poses a huge challenge to the platform's signal processing capability and memory throughput. The digital signal processing of broadband signals requires a large amount of FPGA logic resources, and the ZU47DR used in YunSDR Y750 Neo provides the necessary computing resources for UDC/DDC.

In addition to FPGA resources, the chip also integrates an ARM processor system to meet the needs of high-level algorithms and system scheduling. It also has rich interfaces and can support GUI human-computer interaction interfaces and network control interfaces.

Future wireless systems require stronger computing power to handle increasingly complex algorithms, in which case a single board often cannot meet the requirements and data needs to be transmitted to more powerful computing systems, such as FPGA arrays or computer clusters. High speed fiber optic interfaces have become standard for high-performance SDR systems, and the number and speed of optical ports are key to data transmission bandwidth.

YunSDR Y750Neo uses a 100G optical port as the external data channel of the system. By using the FPGA front-end accelerator card FX200, the 100G optical port has been converted into a PCIe3.0x16 interface, and a comprehensive driver and API interface library is provided. Users can directly call interface functions to obtain data and support full rate communication of the 100G interface. In addition, the FPGA of the FPGA acceleration card adopts an open interface, supporting users to carry out secondary development and achieve algorithm acceleration. The FX200 accelerator card uses Xilinx Kintex UltraScale+series FPGA KU15P as the acceleration chip, and the 16ns process FPGA provides abundant signal processing resources.



COMPARE	Reset	XCKU15P
System Logic Cells (K)		1,143
CLB LUTs (K)		523
DSP Slices		1,968
Memory (Mb)		70.6
GTH 16.3 Gb/s Transceivers		44
GTY 32.75 Gb/s Transceivers		32
I/O Pins		668

Development process support

Support various mainstream development tools and customize FPGA underlying logic according to customer needs, greatly accelerating development progress and allowing customers to focus on implementing differentiated algorithms and systems.

Y750neo Development Kit

1 Software defined radio platform Y750Neo 1



2 5G omnidirectional antenna ANT-1427-5925MHz 4



3 PCIE Accelerator Card FX200 1



4 100G photoelectric cable 1



5 SMA direct cable 4



6 card reader 1



8 USB3.0 data cable 1



10 power adapter 12V11.5A 1



11 National standard power cord 1



7 Data USB flash drive 1



9 TF card 32G 1



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