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AXKU5 Development Board User Manual

Alinx Electronic Limited

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AMD Adaptive Computing Partner PREMIER

Document Revision History

chapter	Revision Overview
V1.0	
all	First version released
V1.1	
2.9: Connector Pin Definitions	1.Corrected the incorrect description of the J1 and J2 connector positions.
V1.2	
2.3: DDR4 3.12: EEPROM 3.13: Temperature Sensor	1.Fixed an error in the description of DDR4 quantity in the introduction; added EEPROM and temperature sensor sections ; 2.Modified the FMC_LA08P/N and RX_CLK pins in the hardware.
V2.0	
3.4: FMC HPC Interface 3.8: 40-pin expansion port	1.Corrected errors in the FPGA pin numbers for the FMCHPC interface and the 40-pin expansion port.
V2.1	
3.3: Gigabit Ethernet interface; 3.4: FMC HPC Interface	1.Adjust the ETH_RXCLK lines of the network port, and add ESD protection to the FMC_LA08_P/N interface;

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Table of Contents

01 Development Board Introduction 5

02 ACKU5 Core Board 7

2.1 Introduction 7

2.2 FPGA Chip 8

2.3 DDR4 9

2.4 QSPI Flash 13

2.5 Clock Configuration 14

2.6 LED lights 16

2.7 Power Supply 16

2.8 Structural Diagram 18

2.9 Connector Pin Definitions 18

03 Expansion board 30

3.1 Introduction 30

3.2 PCIe Slots 30

3.3 Gigabit Ethernet interface 33

3.4 FMC HPC Interface 35

3.5 MIPI Interface 40

3.6 USB to Serial Port 41

3.7 SD Card Slot 42

3.8 40-pin expansion port 43

3.9 Clock Configuration 44

3.10 Buttons and LEDs 46

3.11 JTAG Debug Port 47

3.12 EEPROM 48

3.13 Temperature Sensor 48

3.14 Power Supply 49

3.15 Structural Dimensions Drawing 51

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Alinx Electronic Limited has officially released its development board (model: AXKU5) based on the Xilinx FPGA Kintex Ultrascale+ development platform. To help you quickly understand this development platform, we have compiled this user manual.

Kintex Ultrascale+ FPGA development platform adopts a core board plus expansion board model, which facilitates secondary development and utilization of the core board by users. The core board uses Xilinx's Kintex Ultrascale+ chip xcku5pffvb676 solution , and is equipped with two 1 GB high-speed DDR4 SDRAM chips and two 256Mb QSPI FLASH chips.

The baseboard design provides users with a rich array of peripheral interfaces, including one PCIe 3.0 x 8 interface, one FMC HPC interface, one Gigabit Ethernet interface, one MIPI input interface, one UART serial port interface, one SD card interface, and one 40-pin expansion interface, etc. It can meet users' various requirements for high-speed data exchange, video transmission and processing, and industrial control, making it a "professional-grade " FPGA development platform. It provides possibilities for high-speed data transmission and exchange, data processing, early verification, and later applications. We believe this product is very suitable for students, engineers, and other groups engaged in FPGA development. The image below shows the actual development board.



Figure 1.1.1 - AXKU5 Development Board Diagram

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01 Development Board Introduction

Here is a brief introduction to the features of the Kintex Ultrascale+ AXKU5 development platform.

The development board's overall structure follows our established core board + expansion board design. High-speed inter-board connectors connect the core board and expansion boards.

The core board primarily consists of a minimal system comprised of an XCKU5PFFVB676 chip, two DDR4 memory modules, and a QSPI flash memory module. It utilizes a Xilinx Kintex Ultrascale+ series chip , specifically the XCKU5P - FFVB676-2 -I . Two DDR4 memory chips, each with a capacity of up to 1GB, are connected to the HP port of the FPGA chip, forming a 32-bit data bandwidth. Two 256 Mb QSPI flash memory modules are used for static storage of the FPGA chip's configuration files or other user data.

The baseboard provides a rich set of peripheral interfaces for the core board, including one PCIe 3.0 x 8 interface, one FMC HPC interface, one Gigabit Ethernet interface, one MIPI input interface, one UART serial port interface, one SD card interface, one 40-pin expansion interface, some buttons, and LEDs. The following diagram shows the overall structure of the development system:

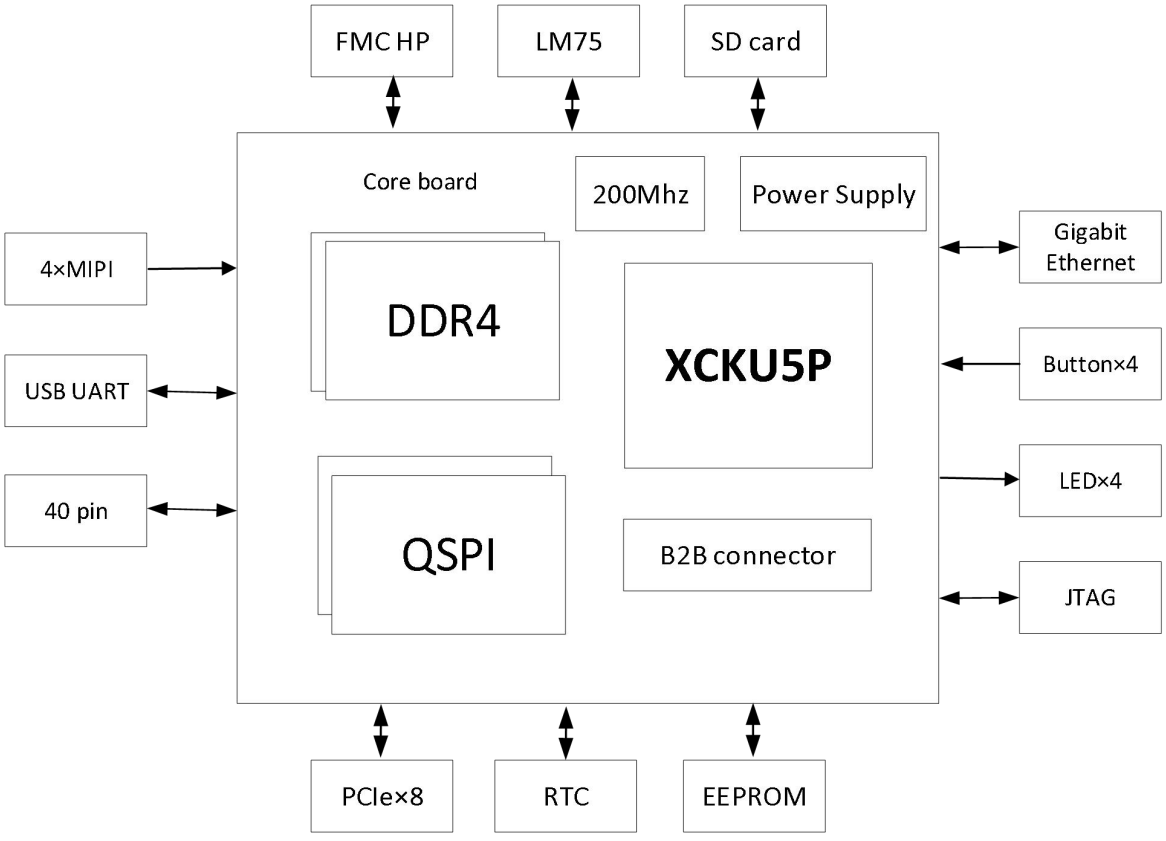

Figure 1.1.2 - Schematic diagram of the development system structure

This diagram shows the interfaces and functions that our development platform can contain.

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- FPGA core board : It consists of a minimum system of XCKU5P + 2 DDR4 + 2 QSPI FLASH, and two crystal oscillators provide clock, with two 200MHz crystal oscillators providing reference clock for FPGA logic and DDR control.
- PCIe 3.0 x 8 interface : Supports the PCI Express 3.0 standard, providing a standard PCIe x 8 high-speed data transmission interface with a single-channel communication rate of up to 8 Gbps .
- 1-channel FMC HPC interface : The 8 high-speed transceivers in the FPGA are connected to the dedicated high-speed pins of FMC HPC, bringing out 34 pairs of LA signal differential pairs and 2 pairs of clock signals of FMC, which can meet the requirements of high-speed signal transmission, comply with the FMC standard, and can be used with various FMC modules (HDMI input/output modules, high-speed AD modules, etc.).
- One Gigabit Ethernet interface : The Gigabit Ethernet interface chip uses the JL2121D Ethernet PHY chip to provide network communication services for users. The chip supports 10/100/1000 Mbps network transmission rates; full-duplex and auto-negotiation.
- 1 MIPI input interface : The board has an onboard 1 MIPI lanex4 input interface with a maximum speed of 2.5Gb/s, which is used to connect MIPI camera modules.
- USB UART Interface : One UART-to-USB interface for communication with a computer, facilitating user debugging. The serial port chip uses the Silicon Labs CP210 2 GM USB- UART chip , and the USB interface uses a MINI USB interface.
- Micro SD Card Slot : 1 Micro SD card slot for storing operating system images and file systems .
- 40-pin expansion port : One 40-pin, 2.54mm pitch expansion port allows connection to various BlackGold modules (dual-lens cameras, TFT LCD screens, high-speed AD modules, etc.). The expansion port includes one 5V power supply, two 3.3V power supply lines, three ground lines, and 34 I/O ports.
- JTAG Debug Port : One 10-pin 2.54mm standard JTAG port for downloading and debugging FPGA programs. Users can debug and download FPGA systems using a Xilinx programmer.
- LEDs : 10 light-emitting diodes (LEDs), 3 on the core board and 7 on the baseboard. The core board has 1 power indicator, 1 DONE configuration indicator, and 1 user indicator. The baseboard has 1 power indicator, 4 user indicators, and 2 serial port indicators.
- Buttons : 4 user buttons on the base plate .

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02 ACKU5 Core Board

2.1 Introduction

The ACKU5 (**core board model, hereinafter the same**) core board uses the Xilinx Kintex Ultrascale+ FPGA chip XCKU5P-FFVB676-2 -I as its main chip. The core board connects two DDR4 memory chips to the FPGA's HP port, forming a 32-bit data bandwidth, with each DDR4 chip having a capacity of up to 1GB. The memory bandwidth on the HP side reaches 85 Gb/s . Additionally, the core board integrates two 256 MB QSPI FLASH chips for boot memory configuration and system files.

This core board utilizes board-to-board connectors to expand to 179 I/O pins. The voltage levels of these I/O pins can be modified by replacing the LDO chip on the baseboard, meeting the requirements of users with different voltage level interfaces. Additionally, the core board also expands to include 16 pairs of high-speed transceiver interfaces. For users requiring a large number of I/O pins, this core board is an excellent choice. Furthermore, the I/O connections feature equal-length and differential traces between the FPGA chip and the interfaces, and the core board's size of only 80*60 (mm) makes it ideal for secondary development.

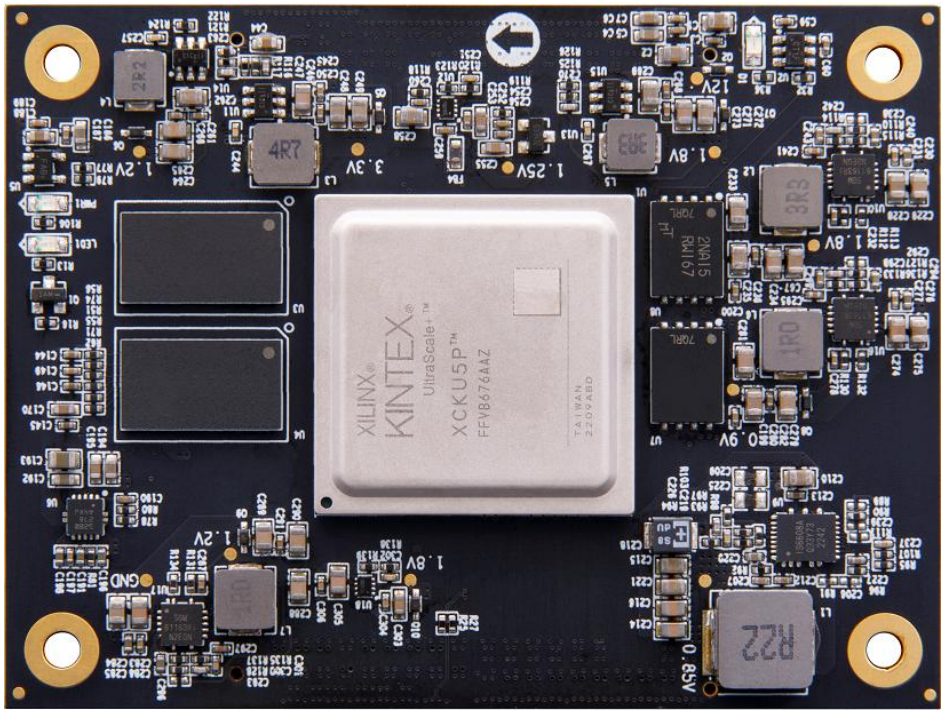

Figure 2.1.1 - Front view of ACKU5 core board

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2.2 FPGA Chip

As previously mentioned, the FPGA we are using is the XCKU5P-FFVB676-2 -I , belonging to Xilinx's Kintex Ultrascale+ series. It has a speed class of 2 and an industrial-grade temperature class. This model is in an FFVB676 package with 676 pins. The naming convention for Xilinx Kintex Ultrascale+ FPGAs is as follows:

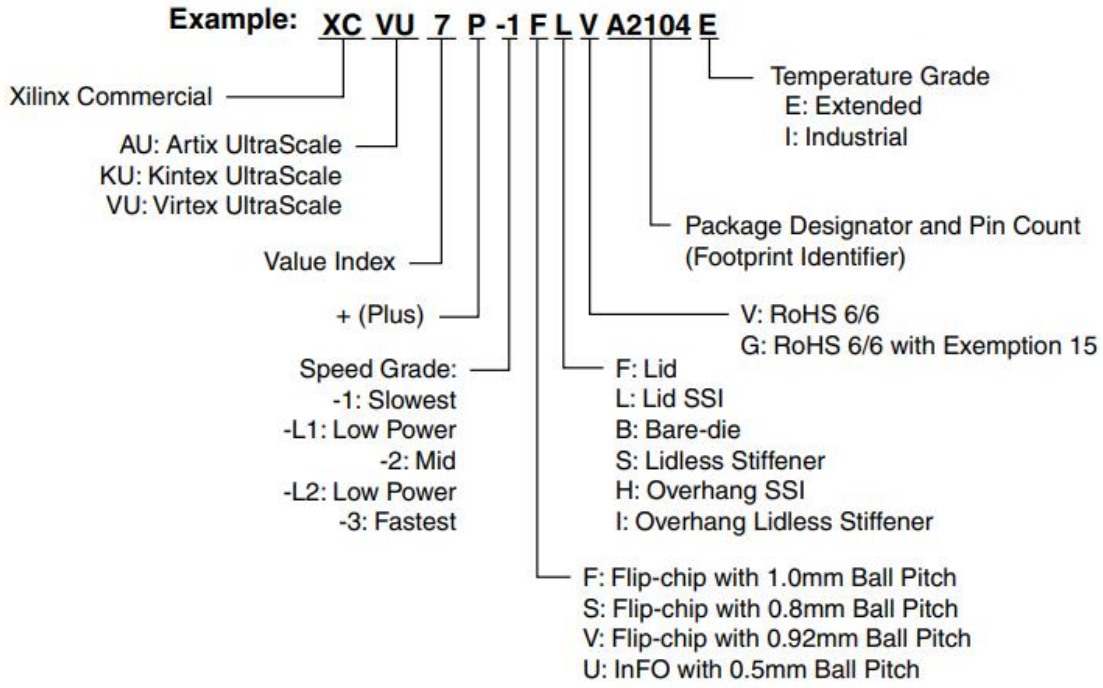

Figure 2.2.1 - Chip Naming Rules

The main parameters of the FPGA chip are shown below:

name	Specific parameters
Logic Cells	475K
Trigger (FF)	433,920
LUTs	216,960
Total Block RAM	16.9 Mb
DSP Slices	1824
CMTs	4
GTY/Gb/s	16/28.21
PCIe Gen3 x16	1

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Speed level	-2
Temperature rating	Industrial grade

Table 2.2.1 - Main Parameters of the Chip

2.3 DDR4

The ACKU5 development board is equipped with two Micron 1GB DDR4 chips , model MT40A512M16LY -062E, connected to the HP side of the FPGA, forming a 32-bit data bus bandwidth and a 2GB capacity. The maximum operating data rate of the DDR4 SDRAM on the FPGA side is 2666Mbps. The two DDR4 memory systems are directly connected to the memory interfaces of BANK 66 and R67 . The specific configuration of the DDR4 SDRAM is shown in the table below.

Position	Chip Model	capacity	factory
U3 , U4	MT40A512M16LY-062E	512M x 16bit	Micron

Table 2.3.1 - DDR 4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. We have fully considered matching resistors/terminating resistors, trace impedance control, and trace length control during circuit and PCB design to ensure the high-speed and stable operation of DDR4.

The hardware connection method of DDR4 on the FPGA side is shown in Figure 2.3.1 :

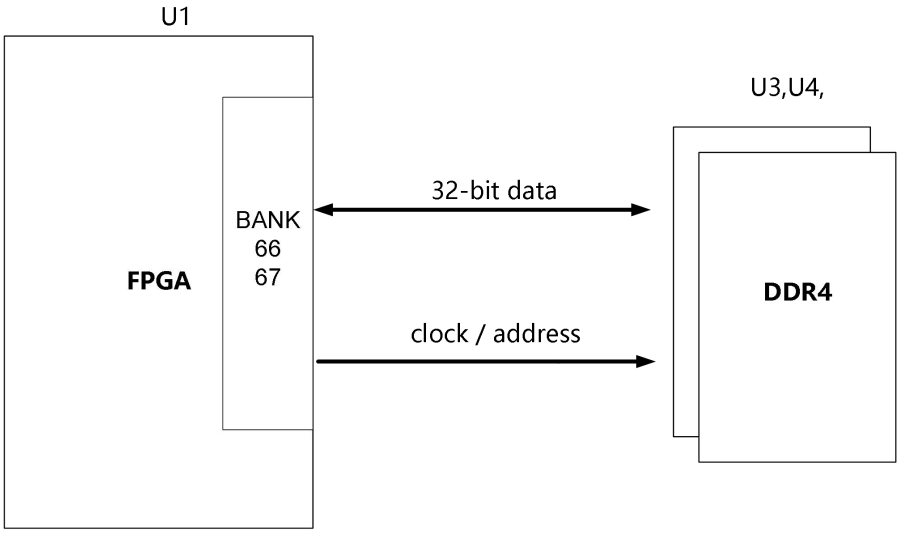

Figure 2.3.1 - Partial Schematic Diagram of DDR4 DRAM

DDR4 SDRAM pin assignment:

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Signal name	pin number
DDR4_D0	C16
DDR4_D1	G16
DDR4_D2	D15
DDR4_D3	G17
DDR4_D4	H17
DDR4_D5	H16
DDR4_D6	D16
DDR4_D7	E15
DDR4_D8	B19
DDR4_D9	C17
DDR4_D10	B20
DDR4_D11	B15
DDR4_D12	A19
DDR4_D13	A15
DDR4_D14	A20
DDR4_D15	B17
DDR4_D16	G20
DDR4_D17	D19
DDR4_D18	D20
DDR4_D19	F19
DDR4_D20	G21
DDR4_D21	E18
DDR4_D22	D18

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DDR4_D23	F18
DDR4_D24	C23
DDR4_D25	C22
DDR4_D26	A24
DDR4_D27	B22
DDR4_D28	A25
DDR4_D29	D21
DDR4_D30	B24
DDR4_D31	E21
DDR4_DM0	G15
DDR4_DM1	C18
DDR4_DM2	H18
DDR4_DM3	A22
DDR4_DQS0_N	E17
DDR4_DQS0_P	E16
DDR4_DQS1_N	A18
DDR4_DQS1_P	A17
DDR4_DQS2_N	E20
DDR4_DQS2_P	F20
DDR4_DQS3_N	B21
DDR4_DQS3_P	C21
DDR4_A0	D26
DDR4_A1	D25
DDR4_A2	E26

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DDR4_A3	C24
DDR4_A4	C26
DDR4_A5	F24
DDR4_A6	M26
DDR4_A7	B25
DDR4_A8	G26
DDR4_A9	B26
DDR4_A10	E25
DDR4_A11	H26
DDR4_A12	D23
DDR4_A13	F25
DDR4_ACT_B	J26
DDR4_BA0	M25
DDR4_BA1	F23
DDR4_BG0	K26
DDR4_CAS_B	E23
DDR4_CKE	L24
DDR4_CLK_N	G25
DDR4_CLK_P	G24
DDR4_CS_B	D24
DDR4_OTD	H24
DDR4_PAR	J25
DDR4_RAS_B	F22
DDR4_RST	L25

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DDR4_WE_B	K25

Table 2.3.1 - DDR4 SDRAM Pin Assignment

2.4 QSPI Flash

The core board is equipped with two 256 MB Quad-SPI FLASH chips, model MT25QU256ABA1EW9-0SIT , which use the 1.8 V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store the FPGA configuration binary file and other user data files. The specific model and related parameters of the QSPI FLASH are shown in the table .

Position	Chip type	capacity	factory
U7, U8	MT25QU256ABA1EW9 -0SIT	256Mbit	Micron

Table 2.4.1 - QSPI Flash Models and Parameters

The QSPI FLASH is connected to dedicated pins on the FPGA chip, with the clock pin connected to CLK of dedicated BANK0, and the data pins connected to BANK0 and BANK65 respectively. The following diagram shows the connection between the QSPI Flash and the FPGA chip.

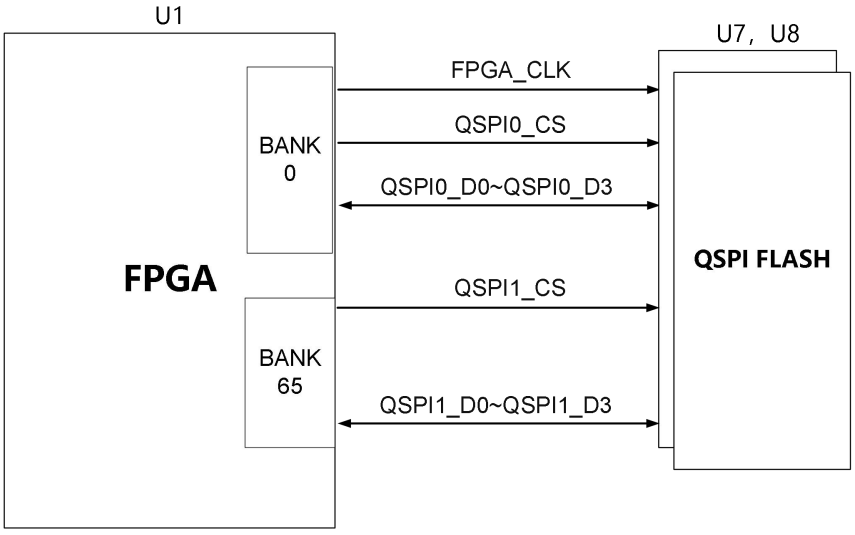

Figure 2.4.1 - QSPI Flash Connection Diagram

Configure chip pin assignments:

Signal name	FPGA pin numbers
QSPI_CLK	Y11
QSPI0_CS	AA12

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QSPI0_DQ0	AD11
QSPI0_DQ1	AC12
QSPI0_DQ2	AC11
QSPI0_DQ3	AE11
QSPI1_CS	U22
QSPI1_DQ0	N23
QSPI1_DQ1	P23
QSPI1_DQ2	R20
QSPI1_DQ3	R21

Table 2.4.2 - QSPI Pin Assignment

2.5 Clock Configuration

The core board provides two 200MHz differential active clocks for the FPGA system. These provide differential clock sources for the FPGA logic sections. A schematic diagram of the clock circuit design is shown below :

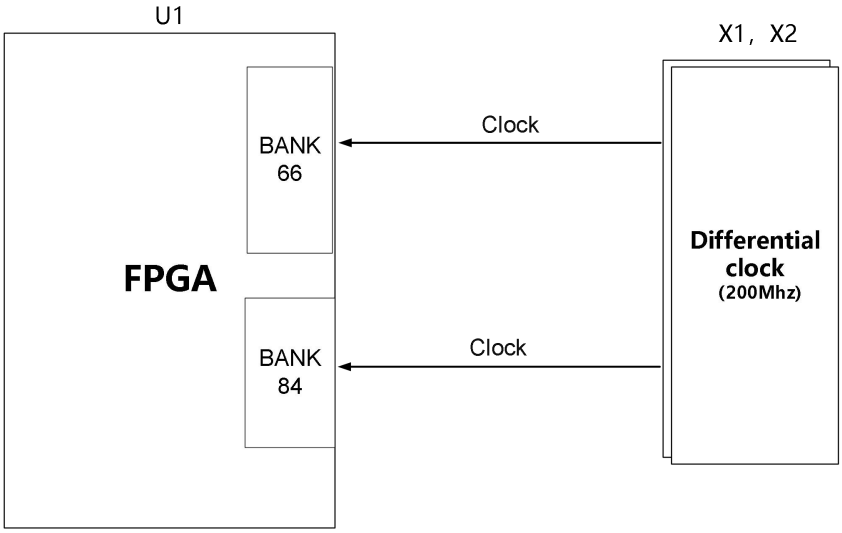

Figure 2.5.1 - Core board clock source

FPGA system clock source

The board provides two 200MHz differential crystal oscillators to provide reference clocks for the DDR4 controller and FPGA logic . The crystal oscillator outputs are connected to the global clocks of FPGAs BANK66 and BANK84, which can be used to drive the DDR4 controller and user logic circuits

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within the FPGA. The schematic diagram of this clock source is shown in the figure .

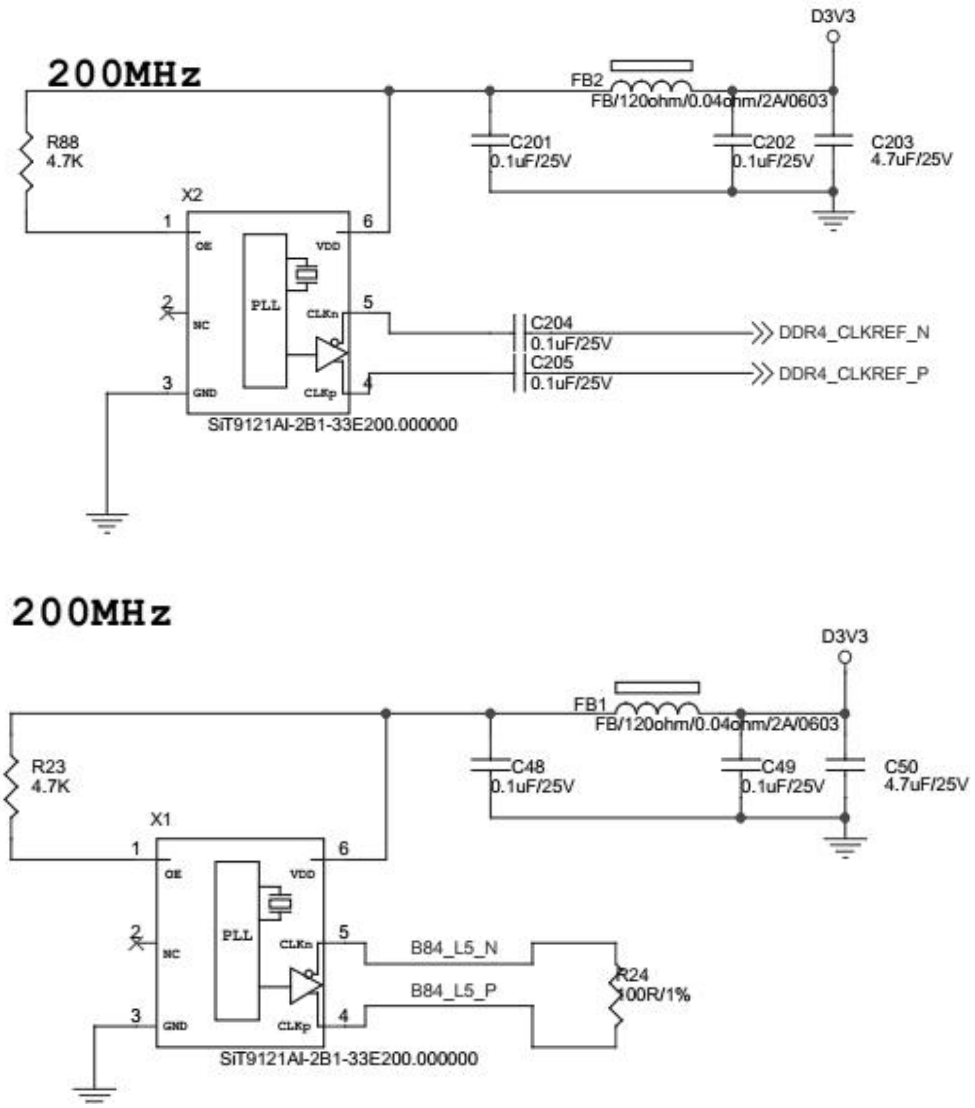

Figure 2.5.2 - System Clock Source

Clock pin assignment:

Signal name	FPGA pins
B84_L5_P	AC13
B84_L5_N	AC14
DDR4_CLKREF_P	K22
DDR4_CLKREF_N	K23

Table 2.5.1 - Clock Pin Assignment

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2.6 LED lights

The ACKU5 core board has three red LEDs: one power indicator (PWR1), one configuration LED (D1), and one user indicator (LED1). The indicator lights up when the core is powered on; the configuration LED lights up after the FPGA configuration program is completed. The user indicator can be used to customize function indications. A schematic diagram of the LED hardware connection is shown in the figure.

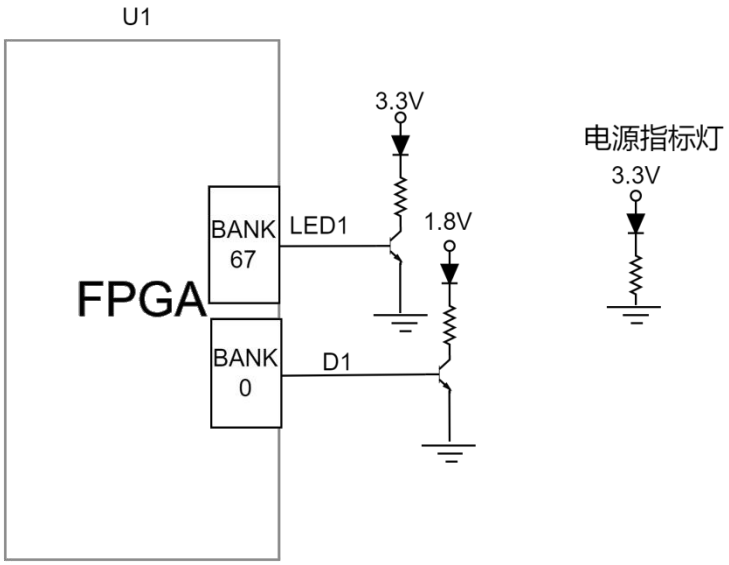

Figure 2.6.1 - Hardware connection diagram of LED lights on the core board

2.7 Power Supply

The ACKU5 core board is powered by +12V and is connected to the baseboard. The power supply design diagram on the board is shown below:

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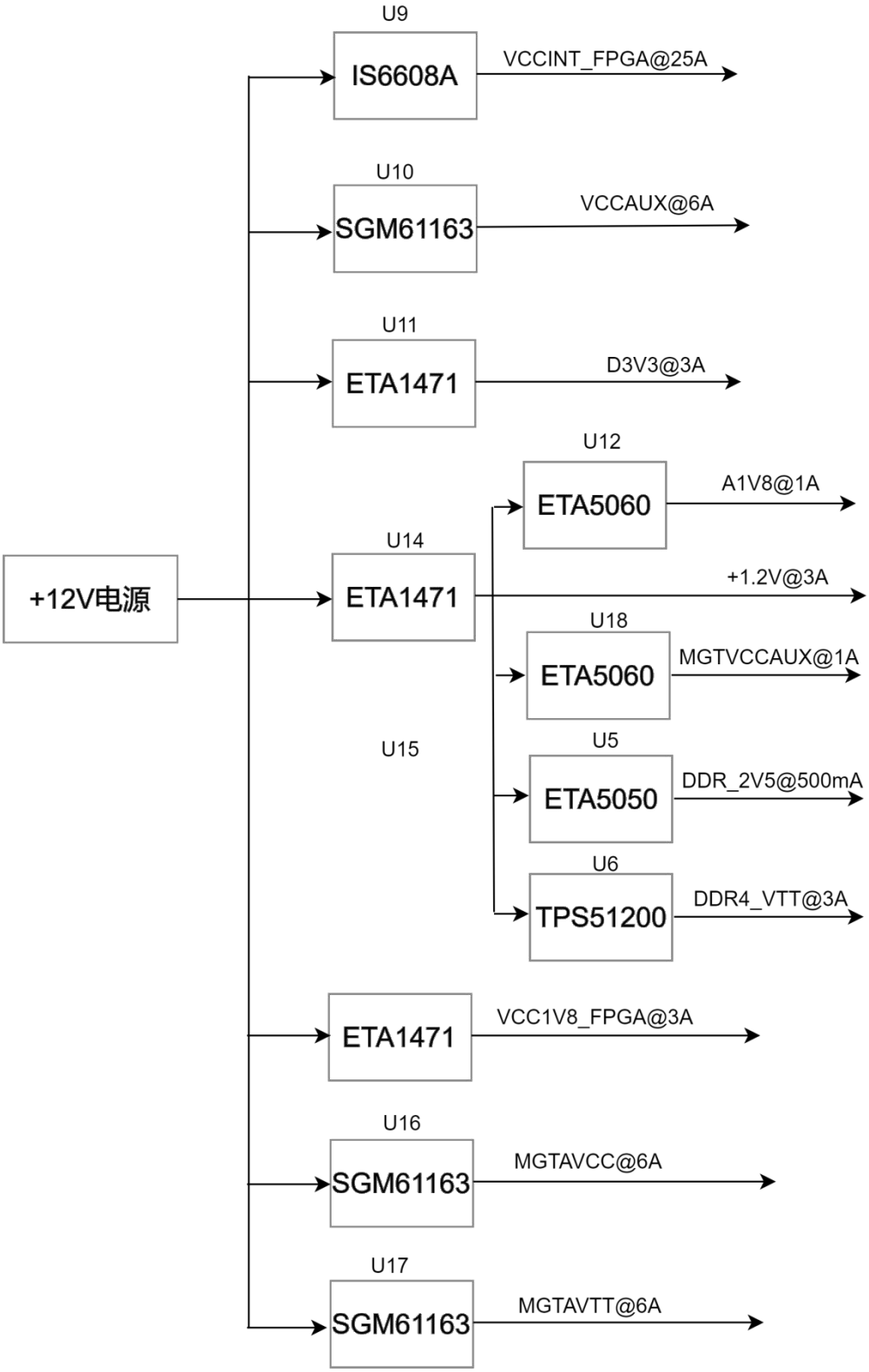

Figure 2.7.1 - Power interface section in the schematic diagram

The +12V power supply generates the FPGA core power supply via the IS6608 DC-DC power chip, with an output current of up to 25A, which can meet the current requirements of the core voltage. The +12V power supply then generates VCCAX, MGTAVCC, and MGTAVTT power supplies via three SGM61163 DC-DC chips to power the FPGA auxiliary power supply and the high-speed

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transceiver. Simultaneously, the +12V power supply generates +1.2V via the ETA1471 DC-DC chip , powering the DDR4, FPGA bank, and peripherals via VCC1V8_FPGA and D3V3. Additionally, the D3V3 generates the auxiliary power supply for the high-speed transceiver and the +1.8V power supply for the FPGA ADC via two ETA5060 LDO chips; the VTT and DDR2V5 voltages for DDR4 are generated by TPS51200 and ETA5050.

Because FPGA power supplies have power-on sequence requirements, we have designed the circuit according to the chip's power requirements to ensure the chip's normal operation.

2.8 Structural Diagram

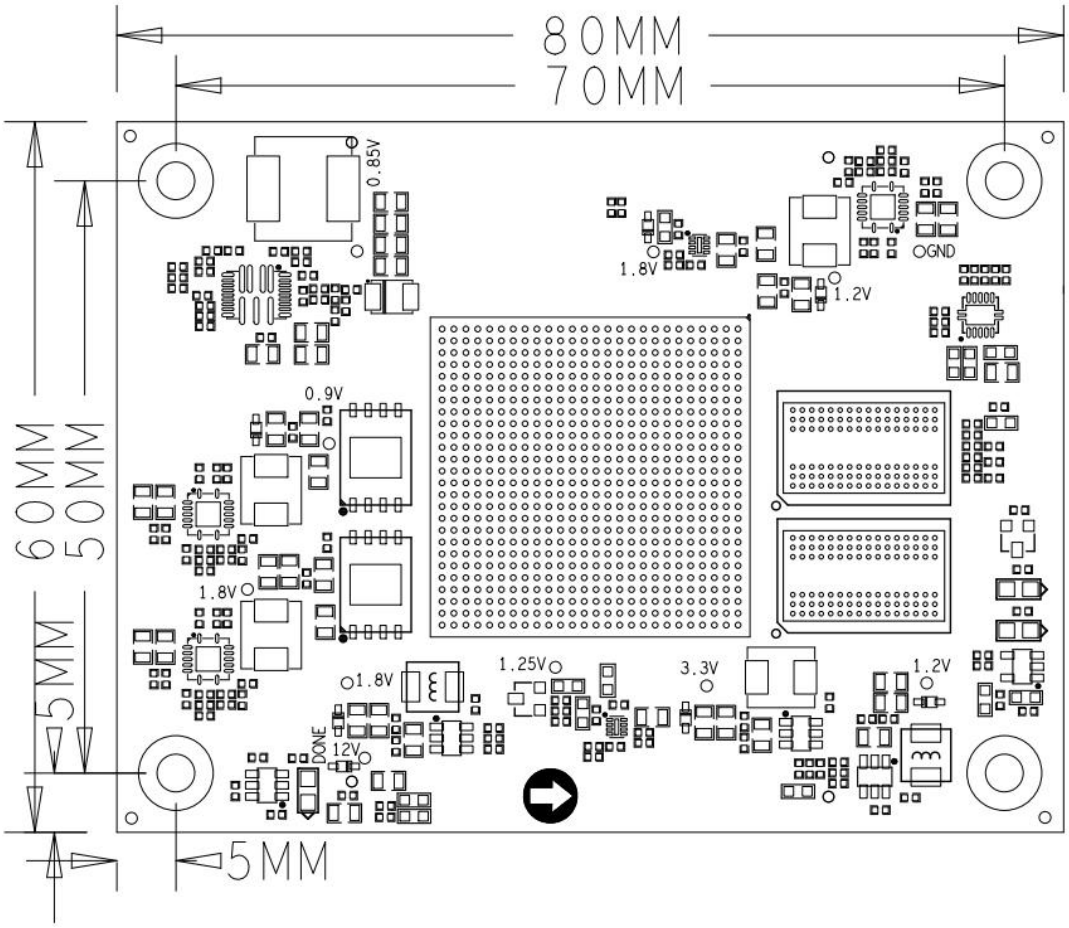

Figure 2.8.1 - Top View

2.9 Connector Pin Definitions

The core board has two high-speed expansion ports, which are connected to the baseboard using two 240-pin inter-board connectors (J1~J2). The core board is powered by the J2 connector.

J1 connector pin assignment

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J1 pin	Signal name	Pin number	J1 pin	Signal name	pin number
A1	POWER_ALT	-	B1	POWER_SDA	-
A2	-	-	B2	POWER_SCL	-
A3	GND	-	B3	GND	-
A4	FPGA_TDI	AB12	B4	FPGA_TCK	AE12
A5	FPGA_TMS	AB10	B5	FPGA_TDO	Y10
A6	GND	-	B6	GND	-
A7	-	-	B7	-	-
A8	-	-	B8	-	-
A9	GND	-	B9	GND	-
A10	-	-	B10	-	-
A11	-	-	B11	-	-
A12	GND	-	B12	GND	-
A13	B87_L3_N	G14	B13	B87_L4_N	J14
A14	B87_L3_P	H14	B14	B87_L4_P	J15
A15	GND	-	B15	GND	-
A16	B87_L2_N	H13	B16	B87_L1_N	H12
A17	B87_L2_P	J13	B17	B87_L1_P	J12
A18	GND	-	B18	GND	-
A19	B87_L5_N	F12	B19	B87_L6_N	F13
A20	B87_L5_P	G12	B20	B87_L6_P	F14
A21	GND	-	B21	GND	-
A22	B87_L7_N	E12	B22	B87_L8_N	D13
A23	B87_L7_P	E13	B23	B87_L8_P	D14

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A24	GND	-	B24	GND	-
A25	B87_L10_N	B12	B25	B87_L11_N	A12
A26	B87_L10_P	C12	B26	B87_L11_P	A13
A27	GND	-	B27	GND	-
A28	B87_L9_N	C13	B28	B87_L12_N	A14
A29	B87_L9_P	C14	B29	B87_L12_P	B14
A30	GND	-	B30	GND	-
A31	GND	-	B31	GND	-
A32	MGT226_CLK0_P	P7	B32	MGT226_CLK1_P	M7
A33	MGT226_CLK0_N	P6	B33	MGT226_CLK1_N	M6
A34	GND	-	B34	GND	-
A35	MGT226_TX0_P	N5	B35	MGT226_RX0_P	M2
A36	MGT226_TX0_N	N4	B36	MGT226_RX0_N	M1
A37	GND	-	B37	GND	-
A38	MGT226_TX1_P	L5	B38	MGT226_RX1_P	K2
A39	MGT226_TX1_N	L4	B39	MGT226_RX1_N	K1
A40	GND	-	B40	GND	-
A41	MGT226_TX2_P	J5	B41	MGT226_RX2_P	H2
A42	MGT226_TX2_N	J4	B42	MGT226_RX2_N	H1
A43	GND	-	B43	GND	-
A44	MGT226_TX3_P	G5	B44	MGT226_RX3_P	F2
A45	MGT226_TX3_N	G4	B45	MGT226_RX3_N	F1
A46	GND	-	B46	GND	-
A47	MGT227_CLK1_P	H7	B47	MGT227_CLK0_P	K7

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A48	MGT227_CLK1_N	H6	B48	MGT227_CLK0_N	K6
A49	GND	-	B49	GND	-
A50	MGT227_TX0_P	F7	B50	MGT227_RX0_P	D2
A51	MGT227_TX0_N	F6	B51	MGT227_RX0_N	D1
A52	GND	-	B52	GND	-
A53	MGT227_TX1_P	E5	B53	MGT227_RX1_P	C4
A54	MGT227_TX1_N	E4	B54	MGT227_RX1_N	C3
A55	GND	-	B55	GND	-
A56	MGT227_TX2_P	D7	B56	MGT227_RX2_P	B2
A57	MGT227_TX2_N	D6	B57	MGT227_RX2_N	B1
A58	GND	-	B58	GND	-
A59	MGT227_TX3_P	B7	B59	MGT227_RX3_P	A4
A60	MGT227_TX3_N	B6	B60	MGT227_RX3_N	A3

Table 2.9.1-J1 Pin Assignment

J1 pin	Signal name	pin number	J1 pin	Signal name	pin numbers
C1	MGT224_TX0_N	AF6	D1	MGT224_RX0_N	AF1
C2	MGT224_TX0_P	AF7	D2	MGT224_RX0_P	AF2
C3	GND	-	D3	GND	-
C4	MGT224_TX1_N	AE8	D4	MGT224_RX1_N	AE3
C5	MGT224_TX1_P	AE9	D5	MGT224_RX1_P	AE4
C6	GND	-	D6	GND	-
C7	MGT224_TX2_N	AD6	D7	MGT224_RX2_N	AD1
C8	MGT224_TX2_P	AD7	D8	MGT224_RX2_P	AD2

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C9	GND	-	D9	GND	-
C10	MGT224_TX3_N	AC4	D10	MGT224_RX3_N	AB1
C11	MGT224_TX3_P	AC5	D11	MGT224_RX3_P	AB2
C12	GND	-	D12	GND	-
C13	MGT224_CLK1_N	Y6	D13	MGT224_CLK0_N	AB6
C14	MGT224_CLK1_P	Y7	D14	MGT224_CLK0_P	AB7
C15	GND	-	D15	GND	-
C16	MGT225_TX0_N	AA4	D16	MGT225_RX0_N	Y1
C17	MGT225_TX0_P	AA5	D17	MGT225_RX0_P	Y2
C18	GND	-	D18	GND	-
C19	MGT225_TX1_N	W4	D19	MGT225_RX1_N	V1
C20	MGT225_TX1_P	W5	D20	MGT225_RX1_P	V2
C21	GND	-	D21	GND	-
C22	MGT225_TX2_N	U4	D22	MGT225_RX2_N	T1
C23	MGT225_TX2_P	U5	D23	MGT225_RX2_P	T2
C24	GND	-	D24	GND	-
C25	MGT225_TX3_N	R4	D25	MGT225_RX3_N	P1
C26	MGT225_TX3_P	R5	D26	MGT225_RX3_P	P2
C27	GND	-	D27	GND	-
C28	MGT225_CLK1_N	T6	D28	MGT225_CLK0_N	V6
C29	MGT225_CLK1_P	T7	D29	MGT225_CLK0_P	V7
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-
C32	-	-	D32	-	-

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C33	-	-	D33	-	-
C34	GND	-	D34	GND	-
C35	-	-	D35	FPGA_VN_IN	R13
C36	-	-	D36	FPGA_VP_IN	P14
C37	GND	-	D37	GND	-
C38	GND	-	D38	GND	-
C39	B86_L2_N	J10	D39	B86_L4_N	G11
C40	B86_L2_P	J11	D40	B86_L4_P	H11
C41	GND	-	D41	GND	-
C42	B86_L3_N	H9	D42	B86_L1_N	K9
C43	B86_L3_P	J9	D43	B86_L1_P	K10
C44	GND	-	D44	GND	-
C45	B86_L9_N	C9	D45	B86_L5_N	G9
C46	B86_L9_P	D9	D46	B86_L5_P	G10
C47	GND	-	D47	GND	-
C48	B86_L6_N	F9	D48	B86_L10_N	A9
C49	B86_L6_P	F10	D49	B86_L10_P	B9
C50	GND	-	D50	GND	-
C51	B86_L7_N	E10	D51	B86_L8_N	D10
C52	B86_L7_P	E11	D52	B86_L8_P	D11
C53	GND	-	D53	GND	-
C54	B86_L11_N	A10	D54	B86_L12_N	B11
C55	B86_L11_P	B10	D55	B86_L12_P	C11
C56	GND	-	D56	GND	-

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C57	-	-	D57	-	-
C58	-	-	D58	-	-
C59	-	-	D59	-	-
C60	-	-	D60	-	-

Table 2.9.2 - J1 Pin Assignment

J2 connector pin assignment

J2 pin	Signal name	pin number	J2 pin	Signal name	pin numbers
A1	+12V	-	B1	+12V	-
A2	-	-	B2	-	-
A3	GND	-	B3	GND	-
A4	VCCIO_65	P22,U23,Y24	B4	VCCIO_64	AA21, AB18, AD22
A5	-	-	B5	-	-
A6	GND	-	B6	GND	-
A7	GND	-	B7	GND	-
A8	-	-	B8	-	-
A9	-	-	B9	-	-
A10	GND	-	B10	GND	-
A11	B84_L2_N	AF13	B11	B84_L1_N	AF15
A12	B84_L2_P	AE13	B12	B84_L1_P	AF14
A13	GND	-	B13	GND	-
A14	B84_L9_N	Y16	B14	B84_L6_N	AB16
A15	B84_L9_P	W16	B15	B84_L6_P	AB15
A16	GND	-	B16	GND	-
A17	B64_L7_N	AF22	B17	B64_L8_N	AE23

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A18	B64_L7_P	AE22	B18	B64_L8_P	AD23
A19	GND	-	B19	GND	-
A20	B64_L3_N	AF25	B20	B64_T2U	AE18
A21	B64_L3_P	AF24	B21	B64_T1U	AF20
A22	GND	-	B22	GND	-
A23	B64_L1_N	AE26	B23	B64_L11_N	AE21
A24	B64_L1_P	AE25	B24	B64_L11_P	AD21
A25	GND	-	B25	GND	-
A26	B64_L4_N	AD26	B26	B64_L5_N	AD25
A27	B64_L4_P	AC26	B27	B64_L5_P	AD24
A28	GND	-	B28	GND	-
A29	B64_L6_N	AC24	B29	B64_L9_N	AC23
A30	B64_L6_P	AB24	B30	B64_L9_P	AC22
A31	GND	-	B31	GND	-
A32	B64_L2_N	AB26	B32	B64_L10_N	AB22
A33	B64_L2_P	AB25	B33	B64_L10_P	AA22
A34	GND	-	B34	GND	-
A35	B64_T3U	AC16	B35	B64_L20_N	AB19
A36	B65_T1U	AA23	B36	B64_L20_P	AA19
A37	GND	-	B37	GND	-
A38	B65_L6_N	W20	B38	B65_L9_N	AA25
A39	B65_L6_P	W19	B39	B65_L9_P	AA24
A40	GND	-	B40	GND	-
A41	B65_L1_N	V19	B41	B65_L8_N	Y26

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A42	B65_L1_P	U19	B42	B65_L8_P	Y25
A43	GND	-	B43	GND	-
A44	B65_L3_N	U20	B44	B65_L5_N	T23
A45	B65_L3_P	T20	B45	B65_L5_P	T22
A46	GND	-	B46	GND	-
A47	B66_L4_N	L19	B47	B65_L19_N	R23
A48	B66_L4_P	M19	B48	B65_L19_P	R22
A49	GND	-	B49	GND	-
A50	B66_L2_N	M21	B50	B65_L16_N	V26
A51	B66_L2_P	M20	B51	B65_L16_P	U26
A52	GND	-	B52	GND	-
A53	B66_L5_N	J21	B53	B65_T3U	T19
A54	B66_L5_P	K21	B54	-	-
A55	GND	-	B55	GND	-
A56	B66_L3_N	J20	B56	B65_L17_N	P26
A57	B66_L3_P	J19	B57	B65_L17_P	P25
A58	GND	-	B58	GND	-
A59	B66_L1_N	K18	B59	B65_L15_N	P24
A60	B66_L1_P	L18	B60	B65_L15_P	N24

Table 2.9.3 - J2 Pin Assignment

J2 pin	Signal name	pin number	J2 pin	Signal name	pin number
C1	+12V	-	D1	+12V	-
C2	-	-	D2	-	-
C3	GND	-	D3	GND	-

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C4	VCCAUX_PG	-	D4	FMC_HPC0_VREF_A_M2C	W18, V18
C5	-	-	D5	-	-
C6	GND	-	D6	GND	-
C7	GND	-	D7	GND	-
C8	B84_L11_N	AA13	D8	B84_L12_N	W13
C9	B84_L11_P	Y13	D9	B84_L12_P	W12
C10	GND	-	D10	GND	-
C11	B84_L3_N	AE15	D11	B84_L10_N	W15
C12	B84_L3_P	AD15	D12	B84_L10_P	W14
C13	GND	-	D13	GND	-
C14	B84_L4_N	AD14	D14	B84_L8_N	AB14
C15	B84_L4_P	AD13	D15	B84_L8_P	AA14
C16	GND	-	D16	GND	-
C17	B64_L17_N	AF17	D17	B84_L7_N	AA15
C18	B64_L17_P	AE17	D18	B84_L7_P	Y15
C19	GND	-	D19	GND	-
C20	B64_L15_N	AF19	D20	B64_L13_N	AE20
C21	B64_L15_P	AF18	D21	B64_L13_P	AD20
C22	GND	-	D22	GND	-
C23	B64_L16_N	AD18	D23	B64_L18_N	AE16
C24	B64_L16_P	AC18	D24	B64_L18_P	AD16
C25	GND	-	D25	GND	-
C26	B64_L14_N	AD19	D26	B64_L22_N	AC17
C27	B64_L14_P	AC19	D27	B64_L22_P	AB17

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C28	GND	-	D28	GND	-
C29	B64_L12_N	AC21	D29	B64_L21_N	AB20
C30	B64_L12_P	AB21	D30	B64_L21_P	AA20
C31	GND	-	D31	GND	-
C32	B64_L24_N	AA18	D32	B64_L23_N	AA17
C33	B64_L24_P	Y18	D33	B64_L23_P	Y17
C34	GND	-	D34	GND	-
C35	-	-	D35	B64_L19_N	Y21
C36	-	-	D36	B64_L19_P	Y20
C37	GND	-	D37	GND	-
C38	-	-	D38	USER_DEF_CLOCK_P	J23
C39	-	-	D39	USER_DEF_CLOCK_N	J24
C40	GND	-	D40	GND	-
C41	B65_L10_N	W26	D41	B65_L12_N	W24
C42	B65_L10_P	W25	D42	B65_L12_P	V24
C43	GND	-	D43	GND	-
C44	B65_L11_N	W23	D44	B65_L7_N	Y23
C45	B65_L11_P	V23	D45	B65_L7_P	Y22
C46	GND	-	D46	GND	-
C47	B65_L4_N	V22	D47	B65_L23_N	P19
C48	B65_L4_P	V21	D48	B65_L23_P	N19
C49	GND	-	D49	GND	-
C50	B65_L20_N	P21	D50	B65_L24_N	N22
C51	B65_L20_P	P20	D51	B65_L24_P	N21

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C52	GND	-	D52	GND	-
C53	B65_L14_N	U25	D53	B65_L13_N	U24
C54	B65_L14_P	T25	D54	B65_L13_P	T24
C55	GND	-	D55	GND	-
C56	B65_T2U	N26	D56	B65_L18_N	R26
C57	B65_L2_P	U21	D57	B65_L18_P	R25
C58	GND	-	D58	GND	-
C59	-	-	D59	-	-
C60	VCCO_84	AC15, Y 1 4	D60	VCCO_86_87	E9,H10, E14,H 1 5

Table 2.9.4 - J2 Pin Assignment

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03 Expansion board

3.1 Introduction

Through the preceding functional overview, we can understand the functions of the expansion board.

- PCIe 3.0 x 8 interface
- 1 gigabit network interface
- 1-channel FMC HPC interface
- 1-channel MIPI input interface
- USB UART interface
- Micro SD Card Slot
- 40-pin expansion port
- JTAG debug port
- LED lights
- button

3.2 PCIe Slots

The AXKU5 expansion board has a PCIe x8 interface that supports the PCIe Gen3.0 protocol. Eight transceivers are connected to the gold fingers of the PCIe x8 for data communication.

The PCIe interface transmits and receives signals directly to the FPGA BANK224 and BANK225 transceivers. The eight TX and RX signals are connected to the FPGA transceivers in a differential signal manner, and the single-channel communication rate can reach up to 8 Gbit bandwidth.

The design schematic of the PCIe interface of the development board is shown in the figure below, where the TX signal is connected using AC coupling mode.

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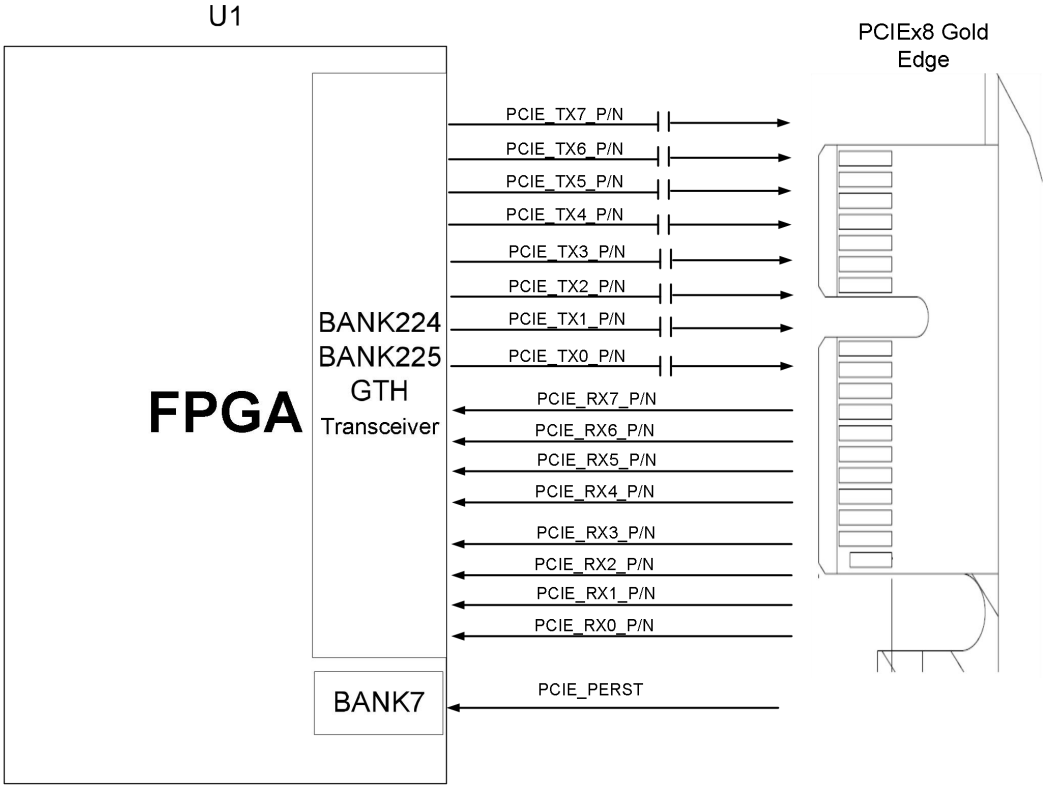

Figure 3.2.1 - Schematic diagram of PCIe slot design

The pin assignments for the PCIe x8 interface FPGA are as follows:

Signal name	pin name	pin numbers	Remark
PCIE_RX0_P	MGT225_RX3_P	P2	PCIe channel 0 data reception is positive.
PCIE_RX0_N	MGT225_RX3_N	P1	PCIe channel 0 data reception negative
PCIE_RX1_P	MGT225_RX2_P	T2	PCIe Channel 1 data reception is positive.
PCIE_RX1_N	MGT225_RX2_N	T1	PCIe Channel 1 Data Receiver
PCIE_RX2_P	MGT225_RX1_P	V2	PCIe Channel 2 data reception is positive
PCIE_RX2_N	MGT225_RX1_N	V1	PCIe Channel 2 Data Receiver
PCIE_RX3_P	MGT225_RX0_P	Y2	PCIe channel 3 data reception is positive
PCIE_RX3_N	MGT225_RX0_N	Y1	PCIe lane 3 data reception negative
PCIe RX4 P	MGT224_RX3_P	AB2	PCIe channel 4 data reception is positive
PCIe RX4 N	MGT224_RX3_N	AB1	PCIe lane 4 data reception negative

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PCIe RX5 P	MGT224_RX2_P	AD2	PCIe channel 5 data reception is positive.
PCIE_RX5_N	MGT224_RX2_N	AD1	PCIe channel 5 data reception negative
PCIE_RX6_P	MGT224_RX1_P	AE4	PCIe channel 6 data reception is positive.
PCIE_RX6_N	MGT224_RX1_N	AE3	PCIe channel 6 data reception negative
PCIe RX7 P	MGT224_RX0_P	AF2	PCIe channel 7 data reception is positive.
PCIE_RX7_N	MGT224_RX0_N	AF1	PCIe lane 7 data reception negative
PCIE_TX0_P	MGT225_TX3_P	R5	PCIe channel 0 data transmission Positive.
PCIE_TX0_N	MGT225_TX3_N	R4	PCIe channel 0 data transmission negative
PCIE_TX1_P	MGT225_TX2_P	U5	PCIe Channel 1 data transmission Positive.
PCIE_TX1_N	MGT225_TX2_N	U4	PCIe Channel 1 Data Transmission Negative
PCIE_TX2_P	MGT225_TX1_P	W5	PCIe Channel 2 data transmission Positive
PCIE_TX2_N	MGT225_TX1_N	W4	PCIe Channel 2 Data Transmission Negative
PCIE_TX3_P	MGT225_TX0_P	AA5	PCIe Channel 3 data transmission Positive
PCIE_TX3_N	MGT225_TX0_N	AA4	PCIe Channel 3 Data Transmission Negative
PCIe TX4 P	MGT224_TX3_P	AC5	PCIe Channel 4 data transmission Positive.
PCIE_TX4_N	MGT224_TX3_N	AC4	PCIe Channel 4 Data Transmission Negative
PCIe TX5 P	MGT224_TX2_P	AD7	PCIe channel 5 data transmission Positive
PCIE_TX5_N	MGT224_TX2_N	AD6	PCIe channel 5 data transmission negative
PCIE_TX6_P	MGT224_TX1_P	AE9	PCIe channel 6 data transmission Positive
PCIE_TX6_N	MGT224_TX1_N	AE8	PCIe channel 6 data transmission negative
PCIE_TX7_P	MGT224_TX0_P	AF7	PCIe channel 7 data transmission Positive.
PCIE_TX7_N	MGT224_TX0_N	AF6	PCIe channel 7 data transmission negative
PCIE_CLK_P	MGT225_CLK0_P	V7	PCIe channel reference clock is positive
PCIE_CLK_N	MGT225_CLK0_N	V6	PCIe channel reference clock negative

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FPGA_PCIE_PERST_N	B65_T3U	T19	PCIe card reset signal

Table 3.2.1 - FPGA Pin Assignment for PCIe x8 Interface

3.3 Gigabit Ethernet interface

The development board uses a JL21221D chip. The Ethernet PHY chip provides network communication services to users. It connects to the FPGA 's I/O interface. The JL21221D chip supports 10/100/1000 Mbps network transmission rates and communicates with the FPGA via the RGMII interface . The JL21221D chip supports MDI/MDX auto-adaptation, various speed auto-adaptation, Master/Slave auto-adaptation, and supports MDIO bus for PHY register management.

The JL21221D detects the voltage levels of specific I/O pins upon power-up to determine its operating mode . (Table 3.3.1) This describes the default settings information of the GPHY chip after power-on.

Configure Pin	illustrate	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 0.01
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3.3.1 - Default Configuration Values for PHY Chip

When the network is connected to Gigabit Ethernet, the FPGA and PHY chip JL2121 communicate via the RGMII bus for data transmission. The transmission clock is 125MHz, and the data is sampled on the rising and falling edges of the clock.

When the network is connected to a 100Mbps Ethernet network, data transmission between the FPGA and the JL2121 PHY chip occurs via the RMII bus, with a transmission clock of 25MHz. Data is sampled on both the rising and falling edges of the clock. The following diagram illustrates the connection between the FPGA and the Ethernet PHY chip:

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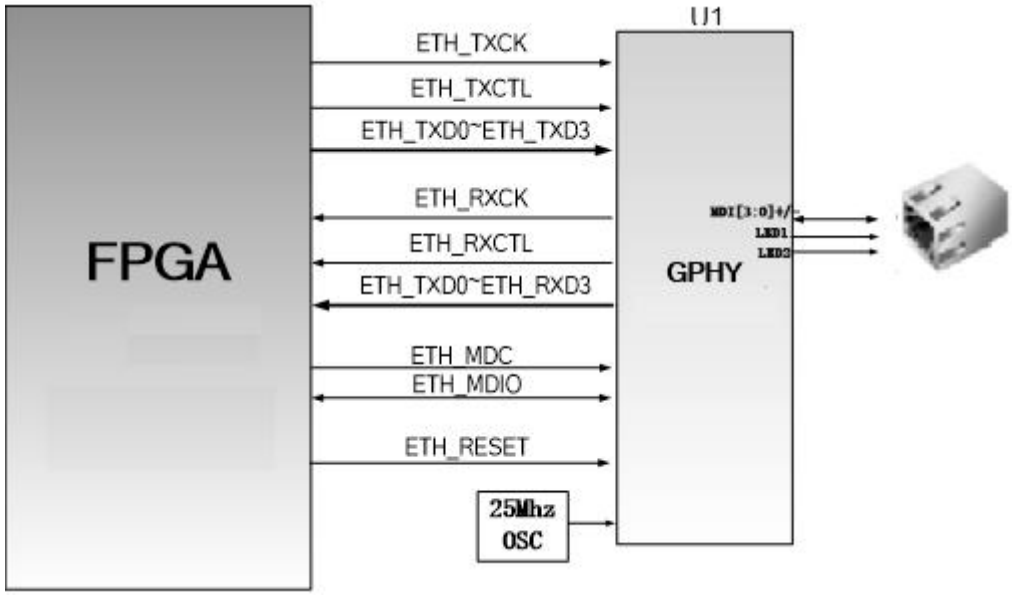

Figure 3.3.1 - Schematic diagram of Gigabit Ethernet interface connection

The FPGA pin assignments for the Ethernet PHY are as follows:

Signal name	pin name	pin numbers	Remark
ETH_MDC	B65_T2U	N26	MDIO manages the clock
ETH_MDIO	B65_L1_P	U19	MDIO Management Data
ETH_RESET	B65_L24_N	N22	PHY chip reset
ETH_RXCK	B65_L11_P	V23	RGMII Receive Clock
ETH_RXCTL	B65_L19_N	R23	Received data valid signal
ETH_RXD0	B65_L1_N	V19	Received data Bit 0
ETH_RXD1	B65_L20_P	P20	Receive data Bit1
ETH_RXD2	B65_L20_N	P21	Receive data Bit 2
ETH_RXD3	B65_L19_P	R22	Receive data Bit 3
ETH_TXCK	B65_L18_P	R25	RGMII Transmit Clock
ETH_TXCTL	B65_L18_N	R26	Send enable signal
ETH_TXD0	B65_L4_P	V21	Send data bit 0
ETH_TXD1	B65_L4_N	V22	Send data bit 1

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ETH_TXD2	B65_L23_P	N19	Send data bit 2
ETH_TXD3	B65_L23_N	P19	Send data bit 3

Table 3.3.2 - FPGA Pin Assignments for Ethernet PHY

3.4 FMC HPC Interface

The development board has one FMC HPC expansion port, which can be connected to various FMC modules from Xilinx or our Alinx (HDMI input/output module, binocular camera module, high-speed AD module, etc.).

The FMC HPC expansion port contains 34 pairs of differential I/O signals, which are connected to the FPGA chips BANK64 and BANK65 respectively, with a default voltage level of 1.8V. Eight high-speed GTY transceiver signals are connected to the I/O pins of the FPGA chips BANK226 and BANK227.

the FPGA and FMC HPC connector is shown in the figure :

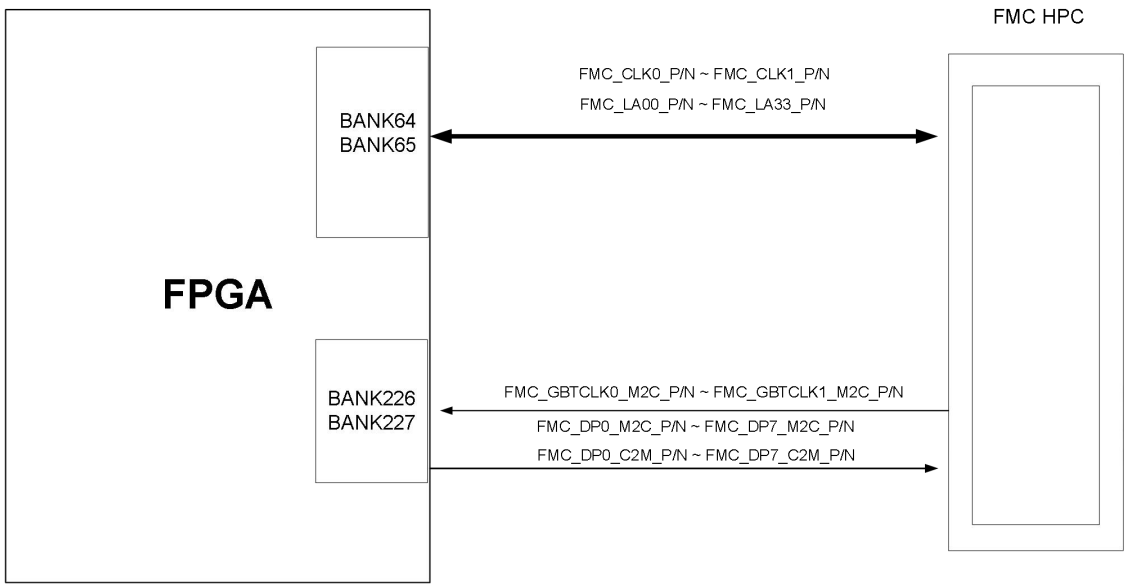

Figure 3.4.1 - HPC FMC Connection Diagram

The pin assignments for the FMC HPC connector are as follows:

signal name	pin name	pin numbers	Remark
FMC_CLK0_N	B65_L12_N	W24	FMC Channel 0 Input Reference Clock N
FMC_CLK0_P	B65_L12_P	V24	FMC Input Reference Clock P (Channel 0)
FMC_CLK1_N	B64_L12_N	AC21	FMC Input Reference Clock N

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FMC_CLK1_P	B64_L12_P	AB21	FMC Input Reference Clock P
FMC_LA00_CC_N	B65_L14_N	U25	FMC LA 0th data (clock) N
FMC_LA00_CC_P	B65_L14_P	T25	FMC LA Channel 0 Data (Clock) P
FMC_LA01_CC_N	B65_L13_N	U24	FMC LA Channel 1 Data (Clock) N
FMC_LA01_CC_P	B65_L13_P	T24	FMC LA Channel 1 Data (Clock) P
FMC_LA02_N	B65_L17_N	P26	FMC LA Second-channel data N
FMC_LA02_P	B65_L17_P	P25	FMC LA Second-Way Data P
FMC_LA03_N	B65_L5_N	T23	FMC LA 3rd channel data N
FMC_LA03_P	B65_L5_P	T22	FMC LA 3rd channel data P
FMC_LA04_N	B65_L16_N	V26	FMC LA 4th data channel N
FMC_LA04_P	B65_L16_P	U26	FMC LA 4th channel data P
FMC_LA05_N	B64_L24_N	AA18	FMC LA 5th data channel N
FMC_LA05_P	B64_L24_P	Y18	FMC LA 5th channel data P
FMC_LA06_N	B65_L10_N	W26	FMC LA 6th channel data P
FMC_LA06_P	B65_L10_P	W25	FMC LA 6th channel data P
FMC_LA07_N	B65_L9_N	AA25	FMC LA 7th data channel N
FMC_LA07_P	B65_L9_P	AA24	FMC LA 7th channel data P
FMC_LA08_N	B65_L3 _N	U20	FMC LA 8th data channel N
FMC_LA08_P	B65_L3 _P	T20	FMC LA 8th channel data P
FMC_LA09_N	B65_L8_N	Y26	FMC LA 9th data channel N
FMC_LA09_P	B65_L8_P	Y25	FMC LA 9th channel data P
FMC_LA10_N	B65_L15_N	P24	FMC LA 10th data channel N
FMC_LA10_P	B65_L15_P	N24	FMC LA 10th data channel P
FMC_LA11_N	B64_L10_N	AB22	FMC LA 11th data channel N

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FMC_LA11_P	B64_L10_P	AA22	FMC LA 11th channel data P
FMC_LA12_N	B65_L7_N	Y23	FMC LA 12th channel data N
FMC_LA12_P	B65_L7_P	Y22	FMC LA 12th channel data P
FMC_LA13_N	B64_L9_N	AC23	FMC LA 13th data channel N
FMC_LA13_P	B64_L9_P	AC22	FMC LA 13th channel data P
FMC_LA14_N	B64_L7_N	AF22	FMC LA 14th data channel N
FMC_LA14_P	B64_L7_P	AE22	FMC LA 14th channel data P
FMC_LA15_N	B64_L11_N	AE21	FMC LA 15th data channel N
FMC_LA15_P	B64_L11_P	AD21	FMC LA 15th channel data P
FMC_LA16_N	B64_L8_N	AE23	FMC LA 16th data channel N
FMC_LA16_P	B64_L8_P	AD23	FMC LA 16th channel data P
FMC_LA17_CC_N	B64_L14_N	AD19	FMC LA 17th data (clock) channel N
FMC_LA17_CC_P	B64_L14_P	AC19	FMC LA 17th data (clock) P
FMC_LA18_CC_N	B64_L13_N	AE20	FMC LA 18th data (clock) channel N
FMC_LA18_CC_P	B64_L13_P	AD20	FMC LA 18th data (clock) channel P
FMC_LA19_N	B64_L18_N	AE16	FMC LA 19th data channel N
FMC_LA19_P	B64_L18_P	AD16	FMC LA 19th channel data P
FMC_LA20_N	B64_L16_N	AD18	FMC LA 20th data channel N
FMC_LA20_P	B64_L16_P	AC18	FMC LA 20th data channel P
FMC_LA21_N	B64_L20_N	AB19	FMC LA 21st data channel N
FMC_LA21_P	B64_L20_P	AA19	FMC LA 21st channel data P
FMC_LA22_N	B64_L21_N	AB20	FMC LA 22nd data channel N
FMC_LA22_P	B64_L21_P	AA20	FMC LA 22nd channel data P
FMC_LA23_N	B64_L23_N	AA17	FMC LA 23rd channel data N

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FMC_LA23_P	B64_L23_P	Y17	FMC LA 23rd channel data P
FMC_LA24_N	B64_L15_N	AF19	FMC LA 24th data channel N
FMC_LA24_P	B64_L15_P	AF18	FMC LA 24th channel data P
FMC_LA25_N	B64_L6_N	AC24	FMC LA 25th data channel N
FMC_LA25_P	B64_L6_P	AB24	FMC LA 25th channel data P
FMC_LA26_N	B64_L19_N	Y21	FMC LA 26th data channel N
FMC_LA26_P	B64_L19_P	Y20	FMC LA 26th data channel P
FMC_LA27_N	B64_L22_N	AC17	FMC LA 27th data channel N
FMC_LA27_P	B64_L22_P	AB17	FMC LA 27th data channel P
FMC_LA28_N	B64_L17_N	AF17	FMC LA 28th data channel N
FMC_LA28_P	B64_L17_P	AE17	FMC LA 28th data channel P
FMC_LA29_N	B64_L1_N	AE26	FMC LA 29th data channel N
FMC_LA29_P	B64_L1_P	AE25	FMC LA 29th data channel P
FMC_LA30_N	B64_L5_N	AD25	FMC LA 30th data channel N
FMC_LA30_P	B64_L5_P	AD24	FMC LA 30th channel data P
FMC_LA31_N	B64_L2_N	AB26	FMC LA 31st data channel N
FMC_LA31_P	B64_L2_P	AB25	FMC LA 31st channel data P
FMC_LA32_N	B64_L4_N	AD26	FMC LA 32nd data channel N
FMC_LA32_P	B64_L4_P	AC26	FMC LA 32nd channel data P
FMC_LA33_N	B64_L3_N	AF25	FMC LA 33rd channel data N
FMC_LA33_P	B64_L3_P	AF24	FMC LA 33rd channel data P
FMC_SCL	B84_L6_P	AB15	FMC I2C bus clock
FMC_SDA	B84_L6_N	AB16	FMC I2C bus data
FMC_HPC_GBTCLK0_M2C_C_N	MGT226_CLK1_N	M6	Transceiver reference clock 0 input P

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FMC_HPC_GBTCLK0_M2C_C_P	MGT226_CLK1_P	M7	Transceiver reference clock 0 input N
FMC_HPC_GBTCLK1_M2C_C_N	MGT227_CLK1_N	H6	Transceiver Reference Clock Input 1 P
FMC_HPC_GBTCLK1_M2C_C_P	MGT227_CLK1_P	H7	Transceiver Reference Clock 1 Input N
FMC_DP0_M2C_P	MGT226_RX0_P	M2	Transceiver data 0 input P
FMC_DP0_M2C_N	MGT226_RX0_N	M1	Transceiver data 0 input N
FMC_DP1_M2C_P	MGT226_RX1_P	K2	Transceiver Data 1 Input P
FMC_DP1_M2C_N	MGT226_RX1_N	K1	Transceiver Data 1 Input N
FMC_DP2_M2C_P	MGT226_RX2_P	H2	Transceiver data 2 input P
FMC_DP2_M2C_N	MGT226_RX2_N	H1	Transceiver data 2 input N
FMC_DP3_M2C_P	MGT226_RX3_P	F2	Transceiver data input 3 P
FMC_DP3_M2C_N	MGT226_RX3_N	F1	Transceiver data 3 inputs N
FMC_DP4_M2C_P	MGT227_RX0_P	D2	Transceiver data 4 input P
FMC_DP4_M2C_N	MGT227_RX0_N	D1	Transceiver data 4 inputs N
FMC_DP5_M2C_P	MGT227_RX1_P	C4	Transceiver data 5 input P
FMC_DP5_M2C_N	MGT227_RX1_N	C3	Transceiver data 5 inputs N
FMC_DP6_M2C_P	MGT227_RX3_P	A4	Transceiver data input 6 P
FMC_DP6_M2C_N	MGT227_RX3_N	A3	Transceiver data 6 inputs N
FMC_DP7_M2C_P	MGT227_RX2_P	B2	Transceiver data input 7 P
FMC_DP7_M2C_N	MGT227_RX2_N	B1	Transceiver data 7 input N
FMC_DP0_C2M_P	MGT226_TX0_P	N5	Transceiver data 0 output P
FMC_DP0_C2M_N	MGT226_TX0_N	N4	Transceiver data 0 output N
FMC_DP1_C2M_P	MGT226_TX1_P	L5	Transceiver Data 1 Output P
FMC_DP1_C2M_N	MGT226_TX1_N	L4	Transceiver data 1 output N
FMC_DP2_C2M_P	MGT226_TX2_P	J5	Transceiver data 2 output P

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FMC_DP2_C2M_N	MGT226_TX2_N	J4	Transceiver data 2 output N
FMC_DP3_C2M_P	MGT226_TX3_P	G5	Transceiver data 3 output P
FMC_DP3_C2M_N	MGT226_TX3_N	G4	Transceiver data 3 output N
FMC_DP4_C2M_P	MGT227_TX0_P	F7	Transceiver data 4 output P
FMC_DP4_C2M_N	MGT227_TX0_N	F6	Transceiver data 4 output N
FMC_DP5_C2M_P	MGT227_TX1_P	E5	Transceiver data 5 output P
FMC_DP5_C2M_N	MGT227_TX1_N	E4	Transceiver data 5 output N
FMC_DP6_C2M_P	MGT227_TX3_P	B7	Transceiver data 6 output P
FMC_DP6_C2M_N	MGT227_TX3_N	B6	Transceiver data 6 output N
FMC_DP7_C2M_P	MGT227_TX2_P	D7	Transceiver data 7 output P
FMC_DP7_C2M_N	MGT227_TX2_N	D6	Transceiver data 7 output N

Table 3.4.1 - FMC HPC Connector Pin Assignment

3.5 MIPI Interface

The AXKU5 expansion board has one MIPI Lanex4 camera input interface, which connects to the FPGA's BANK66 and BANK84. The connection design diagram is shown in Figure 3.5.1 below :

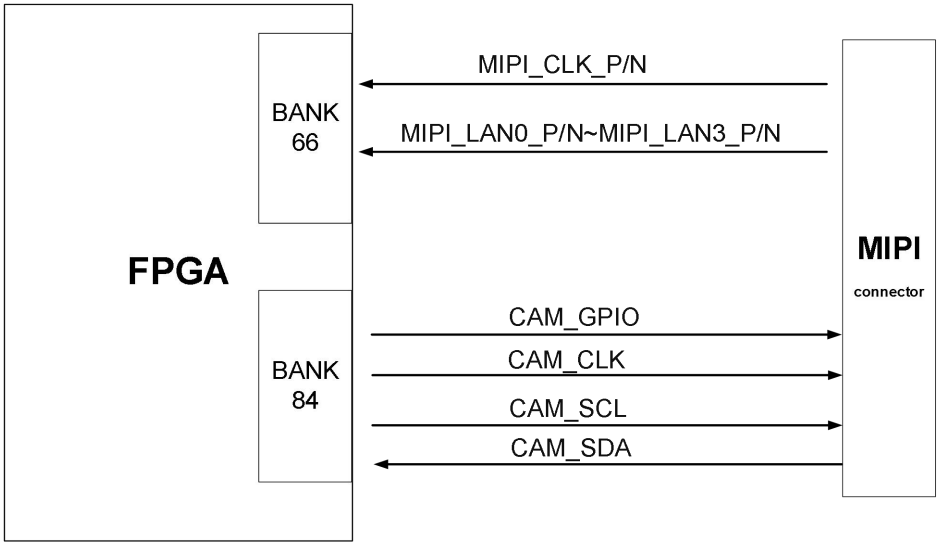

Figure 3.5.1 - MIPI Interface Design Schematic

MIPI Interface Pin Assignment

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Signal name	pin name	pin numbers	Remark
MIPI_CLK_P	B66_L1_P	L18	MIPI input clock positive
MIPI_CLK_N	B66_L1_N	K18	MIPI input clock negative
MIPI_LAN0_P	B66_L5_P	K21	MIPI input data LANE0 is positive
MIPI_LAN0_N	B66_L5_N	J21	MIPI input data LANE0 negative
MIPI_LAN1_P	B66_L2_P	M20	MIPI input data LANE1 is positive
MIPI_LAN1_N	B66_L2_N	M21	MIPI input data LANE1 negative
MIPI_LAN2_P	B66_L3_P	J19	MIPI input data LANE2 is positive
MIPI_LAN2_N	B66_L3_N	J20	MIPI input data LANE2 negative
MIPI_LAN3_P	B66_L4_P	M19	MIPI input data LANE3 is positive
MIPI_LAN3_N	B66_L4_N	L19	MIPI input data LANE3 negative
MIPI_CLK	B84_L10_P	W14	Camera clock input
MIPI_GPIO	B84_L10_N	W15	Camera GPIO control
MIPI_I2C_SCL	B84_L8_N	AB14	Camera I2C clock
MIPI_I2C_SDA	B84_L8_P	AA14	I2C data from the camera

Table 3.5.1 - MIPI Interface Pin Assignment

3.6 USB to Serial Port

The AXKU5 expansion board is equipped with a UART-to-USB interface for system debugging. The converter chip is the Silicon Labs CP2102-GM USB- UART chip , and the USB interface is a MINI USB interface. It can be connected to a PC's USB port using a single USB cable for independent power supply and serial data communication to the core board. A schematic diagram of the USB UART circuit design is shown below :

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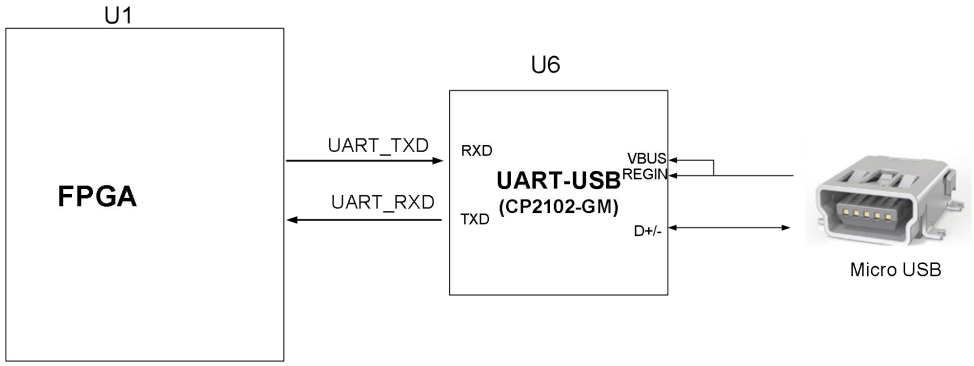

Figure 3.6.1 - Schematic diagram of USB to serial port adapter

FPGA pin assignment for USB to serial port conversion:

Signal name	pin name	pin numbers	Remark
UART_RXD	B84_L3_N	AE15	UART data input
UART_TXD	B84_L3_P	AD15	UART data output

Table 3.6.1 - USB to Serial Port Pin Assignment

3.7 SD Card Slot

The AXKU5 baseboard includes a MicroSD card interface for user access to SD card storage for user data files. The SDIO signal is connected to the FPGA's I/O signals , supporting both SPI and SD modes, and uses a MicroSD card. The schematic diagram of the FPGA and SD card connector is shown in Figure 3.7.1 .

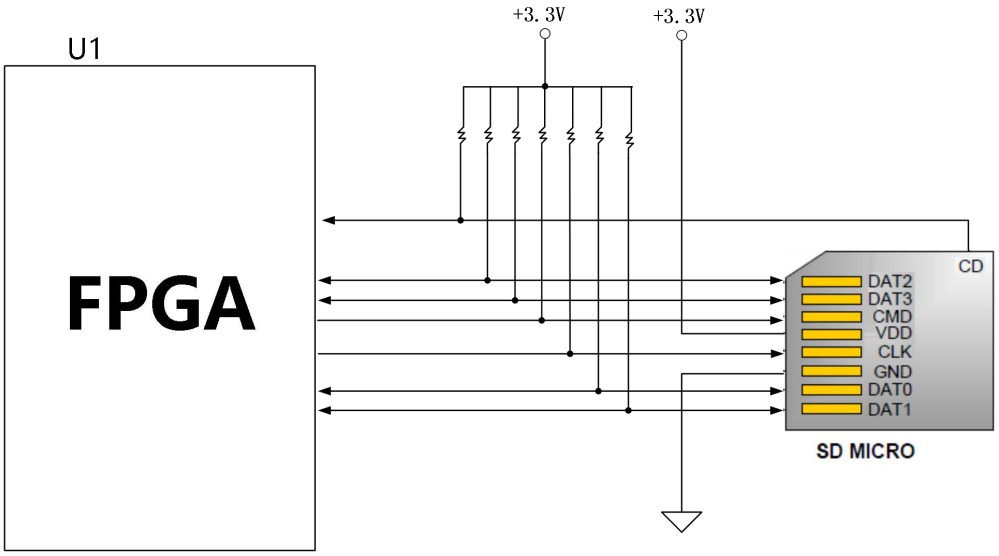

Figure 3.7.1 - SD Card Slot Schematic Diagram

SD card slot pin assignment

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Signal name	pin name	pin numbers	Remark
SD_CD	B84_L4_N	AD14	SD chip select signal
SD_CLK	B84_L11_P	Y13	SD clock signal
SD_CMD	B84_L11_N	AA13	SD command signals
SD_D0	B84_L12_N	W13	SD Data0
SD_D1	B84_L12_P	W12	SD Data Data1
SD_D2	B84_L1_N	AF15	SD Data Data2
SD_D3	B84_L1_P	AF14	SD Data Data3

Table 3.7.1 - SD Card Slot Pin Assignment

3.8 40-pin expansion port

The baseboard has a 40-pin expansion port J8 with a standard 2.54mm pitch, used to connect various modules of the Alinx series or user-designed external circuits. The expansion port has 40 signals, including one 5V power supply, two 3.3V power supply, three ground lines, and 34 I/O ports. The I/O pins of the expansion port are connected to the FPGA's I/O pins, which are set to 3.3V by default.

The pin assignments for the J8 expansion port FPGA are as follows:

J8 pin	Signal name	pin number	J8 pin	Signal name	pin number
1	GND	-	2	+5V	-
3	IO1_1N	A10	4	IO1_1P	B10
5	IO1_2N	B11	6	IO1_2P	C11
7	IO1_3N	E10	8	IO1_3P	E11
9	IO1_4N	A9	10	IO1_4P	B9
11	IO1_5N	D10	12	IO1_5P	D11
13	IO1_6N	C9	14	IO1_6P	D9
15	IO1_7N	F9	16	IO1_7P	F10

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17	IO1_8N	G9	18	IO1_8P	G10
19	IO1_9N	H9	20	IO1_9P	J9
21	IO1_10N	J10	22	IO1_10P	J11
23	IO1_11N	G11	24	IO1_11P	H11
25	IO1_12N	K9	26	IO1_12P	K10
27	IO1_13N	C13	28	IO1_13P	C 14
29	IO1_14N	E12	30	IO1_14P	E13
31	IO1_15N	F12	32	IO1_15P	G12
33	IO1_16N	A12	34	IO1_16P	A13
35	IO1_17N	B12	36	IO1_17P	C12
37	GND	-	38	GND	-
39	+3.3V	-	40	+3.3V	-

Table 3.8.1 - J8 Expansion Port Pin Assignment

3.9 Clock Configuration

The AXKU5 baseboard has two differential active clocks, G2 and G3, with frequencies of 156.25MHz and 125MHz respectively. These provide reference clocks for the FPGA's high-speed transceiver. A schematic diagram of the clock circuit is shown in Figure 3.9.1 below .

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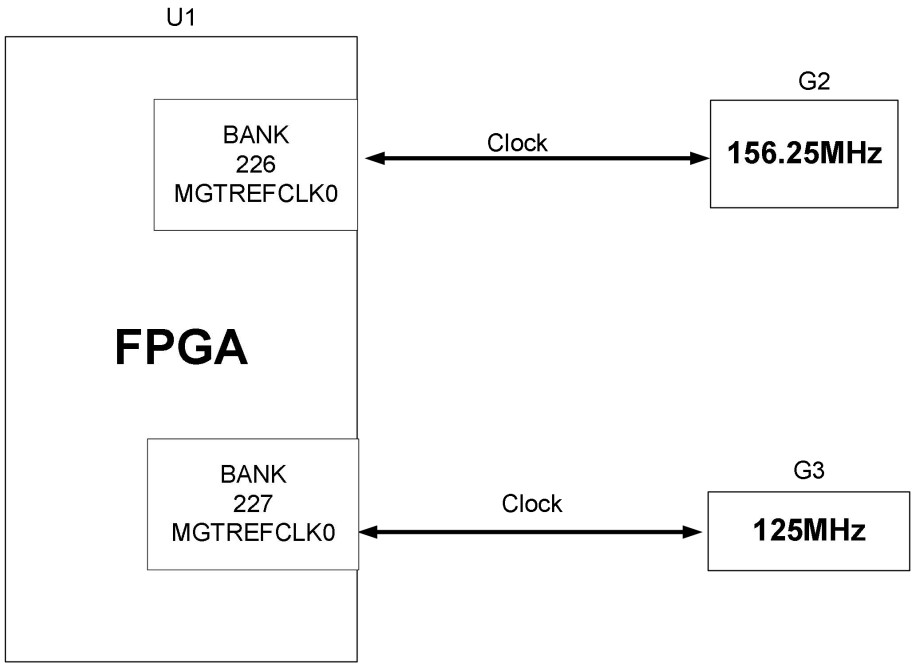

Figure 3.9.1 - Schematic diagram of clock circuit

Clock pin assignment:

Signal name	FPGA pins
MGT_A_CLOCK_P	P7
MGT_A_CLOCK_N	P6
MGT_B_CLOCK_P	K7
MGT_B_CLOCK_N	K6

Table 3.9.1 Clock Pin Assignment

The on-board clock circuit design is shown in Figure 3.9.2 :

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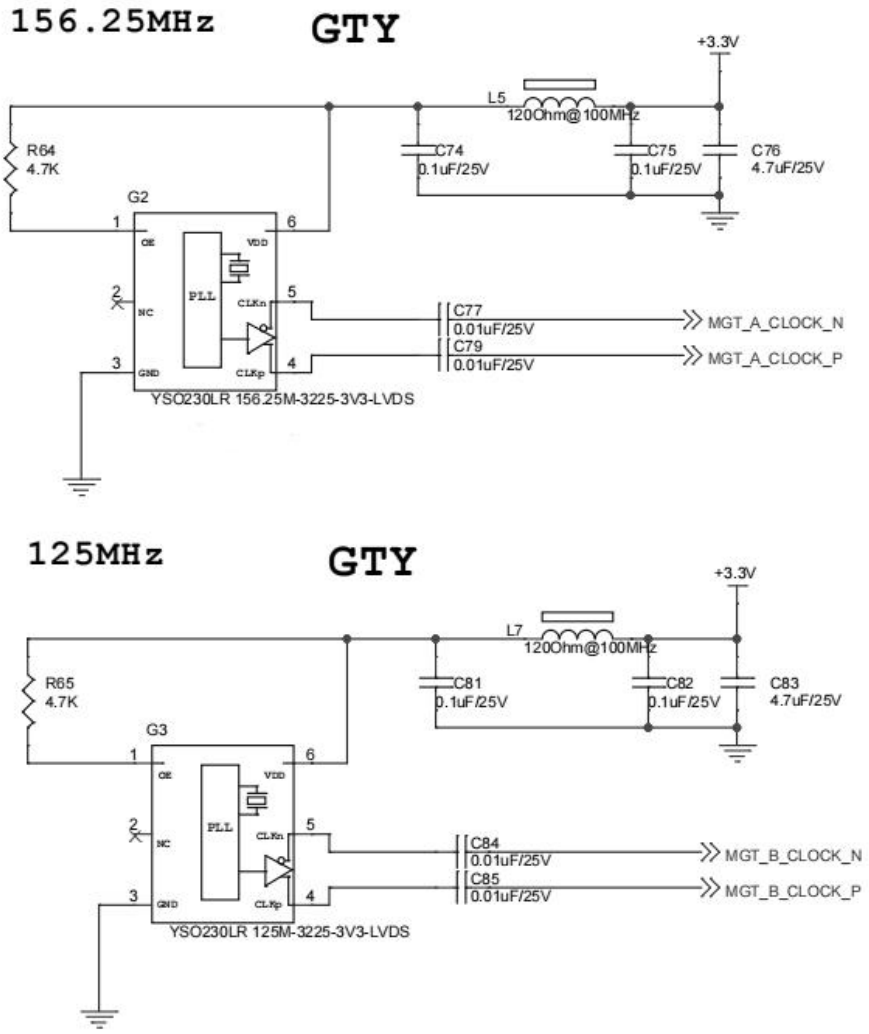

Figure 3.9.2 - System Clock Source

3.10 Buttons and LEDs

The AXKU5 baseboard has 7 LEDs, 1 power indicator, 2 serial communication indicator lights, and 4 user LEDs. The power indicator light illuminates when the development board is powered on. The 4 LEDs are connected to the FPGA's I/O pins, allowing users to control their on/off state via a program. When the I/O voltage connected to a user LED is high, the LED is lit ; when the I/O voltage is low, the LED is off. Additionally, the board has 4 user buttons. The default button signal is high; when a button is pressed, the button signal is low. The hardware connection diagram for the user LEDs and buttons is shown in Figure 3.10.1 .

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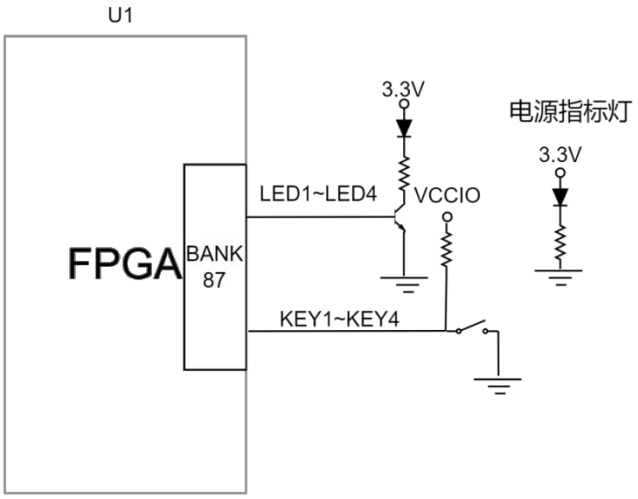

Figure 3.10.1 - Schematic diagram of hardware connection for user LED lights and buttons

Pin assignment for user LEDs and buttons

Signal name	pin name	pin numbers	Remark
KEY1	B87_L4_N	J14	User button 1
KEY2	B87_L4_P	J15	User button 2
KEY3	B87_L2_P	J13	User button 3
KEY4	B87_L2_N	H13	User button 4
LED1	B87_L1_P	J12	User LED1 light
LED2	B87_L3_P	H14	User LED2 lights
LED3	B87_L6_N	F13	User LED 3 lights
LED4	B87_L1_N	H12	User LED 4 lights

Table 3.10.1 - Pin Assignments for User LEDs and Buttons

3.11 JTAG Debug Port

A 10-pin JTAG interface is provided on the AXKU5 baseboard for downloading FPGA programs or burning programs to FLASH. To prevent damage to the FPGA chip from hot-plugging, a protection diode is added to the JTAG signal to ensure that the signal voltage is within the acceptable range for the FPGA, thus avoiding chip damage.

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3.12 EEPROM

The AXKU5 development board features an onboard EEPROM, model 24LC04, with a capacity of 4Kbit (2*256*8bit), consisting of two 256-byte blocks, communicating via the I2C bus. The onboard EEPROM is used to learn the I2C bus communication method. The EEPROM's I2C signal is connected to the FPGA's BANK B1 IO port. Figure 3.12.1 below shows the EEPROM design schematic.

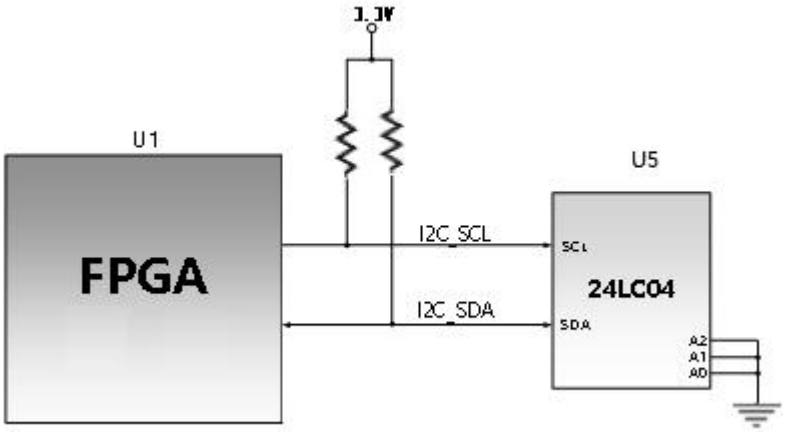

Figure 3.12.1 - EEPROM schematic diagram

EEPROM pin assignment:

Pin Name	FPGA pins
EEPROM_I2C_SCL	AB14
EEPROM_I2C_SDA	AA14

Table 3.12.1 - EEPROM Pin Assignment

3.13 Temperature Sensor

The AXKU5 development board is equipped with a high-precision, low-power digital temperature sensor chip, the ON Semiconductor LM75A. The LM75A chip has a temperature accuracy of 0.125 degrees Celsius. The sensor and FPGA share a direct I2C digital interface; the FPGA reads the temperature near the development board via the I2C interface. Figure 3.13.1 below shows a schematic diagram of the LM75A sensor chip design.

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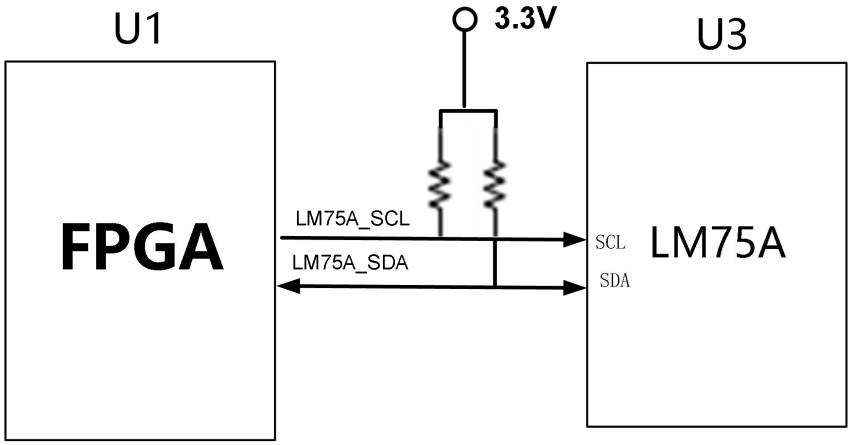

Figure 3.13.1 - Partial schematic diagram of the LM75A sensor

LM75A sensor pin assignment:

Pin Name	FPGA pins
LM75A_SCL	Y15
LM75A_SDA	AA15

Table 3.13.1 - LM75A Sensor Pin Assignment

3.14 Power Supply

The development board's power input voltage is DC 12V, which can be supplied via a PCIe slot or an external +12V power supply. When using an external power supply, please use the power supply provided with the development board; do not use other power supplies to avoid damaging the board. The external power input on the baseboard is output through a voltage protection chip. DC/DC power chips ETA8156, ETA1471, and SGM61163 convert the power into three channels: +5V, +V_ADJ, and +3.3V, respectively. The +3.3V output simultaneously supplies the voltage required by each FPGA bank in the multi-LDO output JTAG. The power supply design schematic on the board is shown in the following figure :

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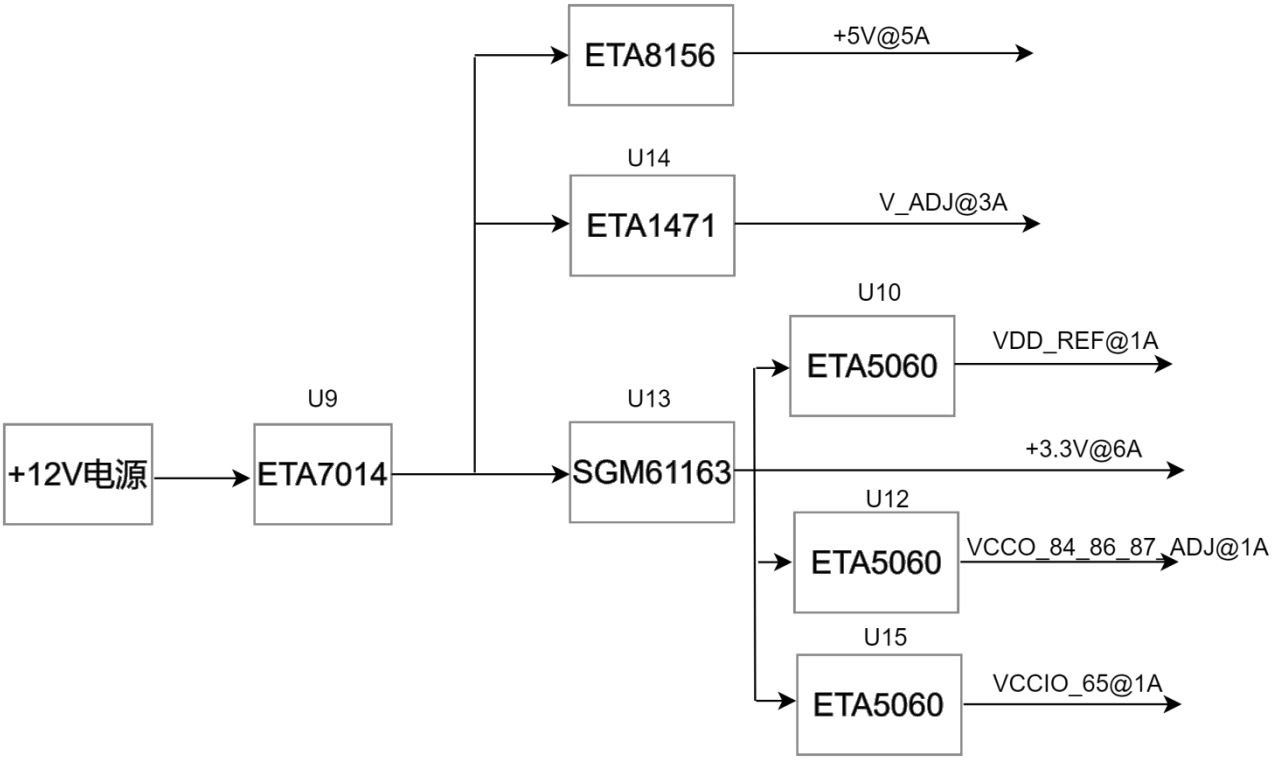

Figure 3.14.1 - Power interface section in the schematic diagram

The functions of each power distribution unit are shown in the table below:

power supply	Function
+5.0V	Expansion module power supply
V_ADJ	FPGA BANK voltage
+3.3V	External power supply for base plate
VDD_REF	JTAG power supply
VCCIO_65	FPGA BANK voltage
VCCO_84_86_87_ADJ	FPGA BANK voltage

Table 3.14.1 - Power Function Allocation

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3.15 Structural Dimensions Drawing

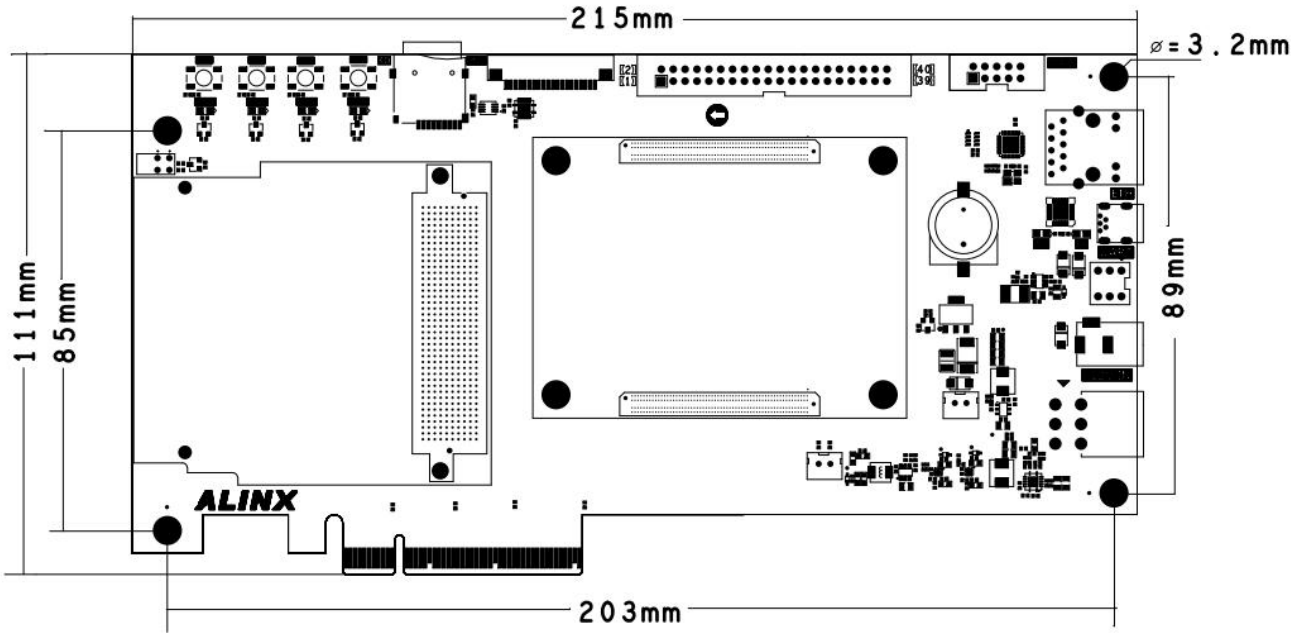

Figure 3.15.1 - Top View

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