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AXKU15S Development Board User Manual

Alinx Electronic Limited

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AMD Adaptive Computing Partner PREMIER

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Alinx Electronic Limited has officially released its development board (model AXKU15S) based on the Xilinx FPGA Kintex Ultrascale+ development platform. To help you quickly understand this platform, we have edited this user manual.

This Kintex Ultrascale+ FPGA development platform adopts SoM(System-on-Module) plus carrier board , which facilitates secondary development and utilization of the SoM by users. The SoM uses Xilinx 's Kintex Ultrascale+ chip XCKU15P-FFVE1517 solution , and is equipped with five 1GB high - speed DDR4 SDRAM chips and two 64MB QSPI FLASH chips.

The carrier board design provides users with a rich array of peripheral interfaces, including one PCIe 3.0 x 16 interface, two FMC HPC interfaces, one Gigabit Ethernet interface, two QSFP28 fiber optic interfaces , two MIPIx4 input interfaces, one UART serial port interface, and one SD card interface, among others. It can meet various high-speed data exchange, video transmission and processing, and industrial control requirements, making it a " professional-grade " FPGA development platform. It provides possibilities for high-speed data transmission and exchange, data processing, early verification, and later applications. We believe this product is very suitable for students, engineers, and other professionals engaged in FPGA development. The image below shows the actual development board.



Figure 1.1.1 - Physical image of the AXKU15S development board

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Chapter 1 Development Board Introduction

The development board's overall structure follows our established SoM + carrier board design. The SoM and carrier boards are connected using high-speed board-to-board connectors.

The SoM primarily consists of a minimum system comprised of an XCKU15P-FFVE1517 chip , five DDR4 memory modules, and a QSPI flash memory module. It utilizes a Xilinx Kintex Ultrascale+ series chip , specifically the XCKU15P-FFVE1517 . Five DDR4 memory chips, each with a capacity of up to 1 GB, are connected to the HP port of the FPGA chip , forming an 80- bit data bus width . Two 64MB QSPI flash memory modules are used for static storage of the FPGA chip's configuration files or other user data.

The carrier board provides a rich set of peripheral interfaces for the SoM, including one PCIe 3.0 x16 interface, two FMC HPC interfaces, one Gigabit Ethernet interface, two MIPI input interfaces, one UART serial port interface, one SD card interface , some buttons and LEDs.

The following diagram shows the overall structure of the development system:

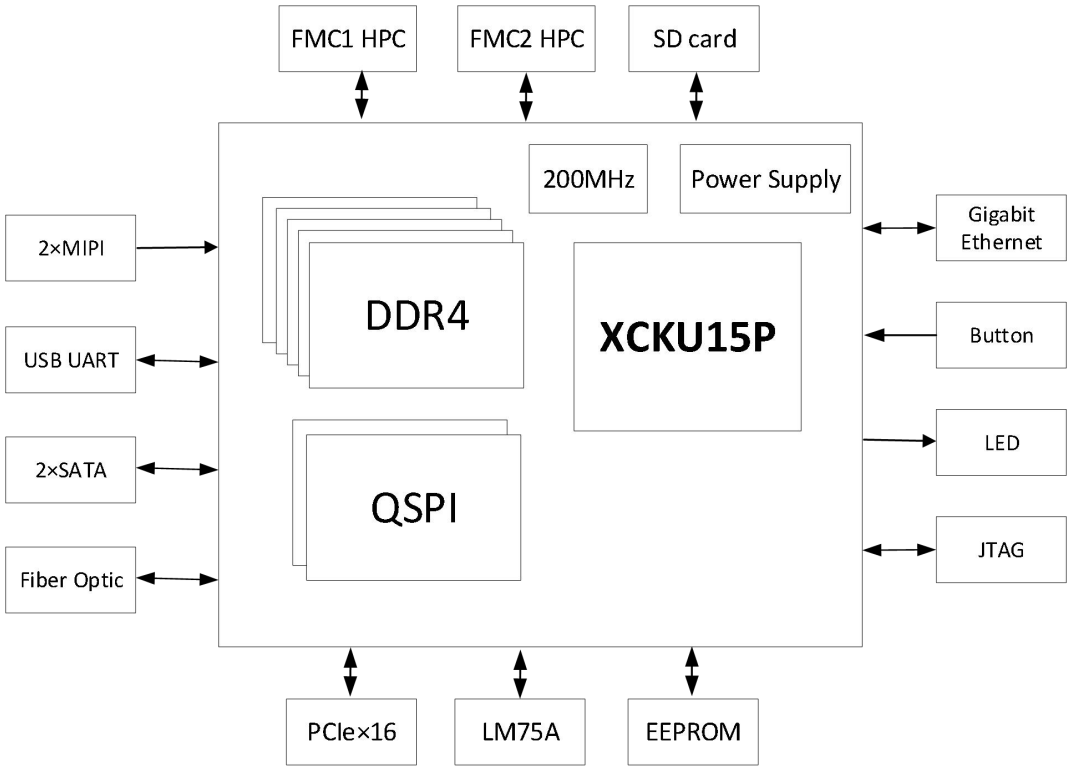


Figure 1.1.2 - Schematic diagram of the development system structure

This diagram shows the interfaces and functions that our development platform can contain.

- FPGA SoM : Comprises a minimal system based on the XCKU15P, five DDR4 memory modules, and two QSPI Flash chips; it also features two oscillators for timing, with two 200MHz oscillators providing reference clocks for the FPGA logic and DDR controllers.

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- PCIe 3.0 x16 interface : Supports PCI Express 3.0 standard, provides standard PCIe x16 high-speed data transmission interface, and single-channel communication rate can reach up to 8 Gbps .
- Two FMC HPC interfaces : The eight high-speed transceivers in the FPGA are connected to the dedicated high-speed pins of the FMC HPC . One FMC interface leads out 34 pairs of LA signal differential pairs, 2 pairs of clock signals, and 24 pairs of HA signals; the other FMC interface leads out 34 pairs of LA signal differential pairs and 2 pairs of clock signals, which can meet the requirements of high-speed signal transmission, comply with the FMC standard, and can be used with various FMC modules (HDMI input/output modules, high-speed AD modules, etc.).
- One Gigabit Ethernet interface: The Gigabit Ethernet interface chip uses the JL2121D Ethernet PHY chip to provide network communication services for users. The chip supports 10/100/1000 Mbps network transmission rates , full-duplex, and auto-negotiation.
- 2-channel MIPI input interface: Onboard 2-channel MIPI lanex4 input interface, supporting a maximum speed of 2.5Gb/s, for connecting MIPI camera modules .
- USB UART Interface : One UART-to-USB interface for communication with a computer, facilitating user debugging. The serial port chip uses the Silicon Labs CP2102N USB-UART chip , and the USB interface uses a MINI USB interface.
- Micro SD Card Slot : 1 Micro SD card slot for storing operating system images and file systems .
- 2 SATA interfaces:Two standard SATA interfaces that can be used to connect SATA peripherals, such as SATA interface solid-state drives .
- JTAG Debug Port: One 10-pin 2.54mm standard JTAG port for downloading and debugging FPGA programs. Users can debug and download FPGA systems using a Xilinx programmer.
- LEDs : 10 LEDs, 3 on the SoM and 7 on the carrier board . The SoM has 1 power indicator, 1 DONE configuration indicator , and 1 user indicator. The carrier board has 1 power indicator, 4 user indicators, and 2 serial port indicators.
- Buttons : 4 user buttons on the carrier board .

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Chapter 2 ACKU15S SoM

2.1 Introduction

The ACKU15S (SoM model, same below) SoM uses an FPGA chip based on Xilinx. The design utilizes the XCKU15P-FFVE1517 main chip from the Kintex Ultrascale+ FPGA . The SoM connects five DDR4 memory chips to the FPGA's HP port, forming an 80- bit data bandwidth. Each DDR4 chip has a capacity of up to 1 GB , and the maximum operating data rate of DDR is 2666 Mbps . Additionally, the SoM integrates two 64MB QSPI FLASH chips for boot memory configuration and system files.

This SoM utilizes four board-to-board connectors to expand to 236 HP I/Os and 88 HD I/Os . The I/O voltage levels can be modified by replacing the LDO chip on the carrier board to meet the different voltage level requirements. Additionally, the SoM also expands to include 24 pairs of GTY and 32 pairs of GTH high-speed transceiver interfaces. For users requiring a large number of I/Os and high-speed transceivers , this SoM is an excellent choice. Furthermore, the I/O connections feature equal-length and differential routing between the FPGA chip and the interfaces, and the SoM's dimensions of only 80* 80 (mm) make it ideal for secondary development.



Figure 2.1.1 - Front view of ACKU15S SoM

2.2 FPGA Chip

The FPGA model we adopt is XCKU15P-FFVE1517 with speed grade 2 and industrial

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temperature grade, packaged in FFVE1517 form factor featuring 1517 pins. The chip naming convention is as follows:

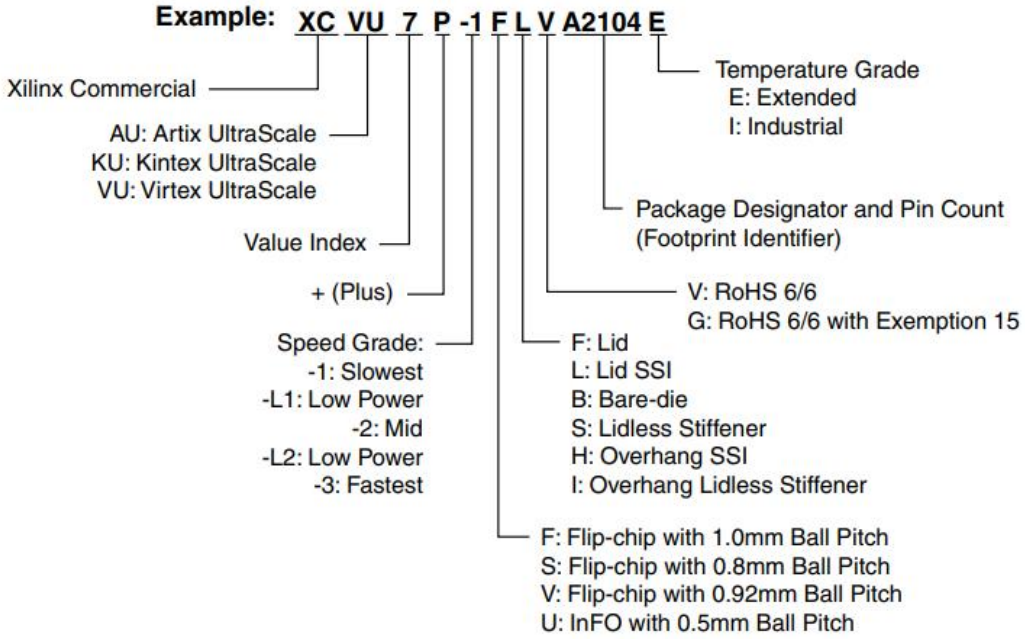


Figure 2.2.1 - Chip naming rules .

The main parameters of the FPGA chip are shown below:

Parameter	Specific parameters
Logic Cells	1143K
Trigger (FF)	1,045,440
LUTs	522,720
Total Block RAM	34.6 Mb
DSP Slices	1968
CMTs	11
GTY/Gb/s	24/ 28Gb/s
GTH/Gb/s	32/16Gb/s
PCIe Gen3 x 16	1
Speed level	- 2
Temperature rating	Industrial grade

Table 2.2.1 - Main Parameters of the Chip

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2.3 DDR4

The ACKU15S development board is equipped with five Nanya (NT5AD512M16C4-HR) 1GB DDR4 chips , connected to the FPGA's HP side, forming an 80 - bit data capacity of 5GB . The DDR4 SDRAM's maximum operating data rate on the FPGA side is 2666 Mbps. The five DDR4 memory chips are directly connected to the bank 66 , 67, 68. The specific configuration of DDR4 SDRAM is shown in the table below.

Position	Chip Model	Capacity	Factory
U3 , U4 , U7, U8, U9	NT5AD512M16C4-HR	1GB	Nanya

Table 2.3.1 - DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. During circuit and PCB design, we have fully considered matching resistors/terminating resistors, trace impedance control, and trace length control to ensure the high-speed and stable operation of DDR4. The hardware connection method of DDR4 on the FPGA side is shown in the figure:

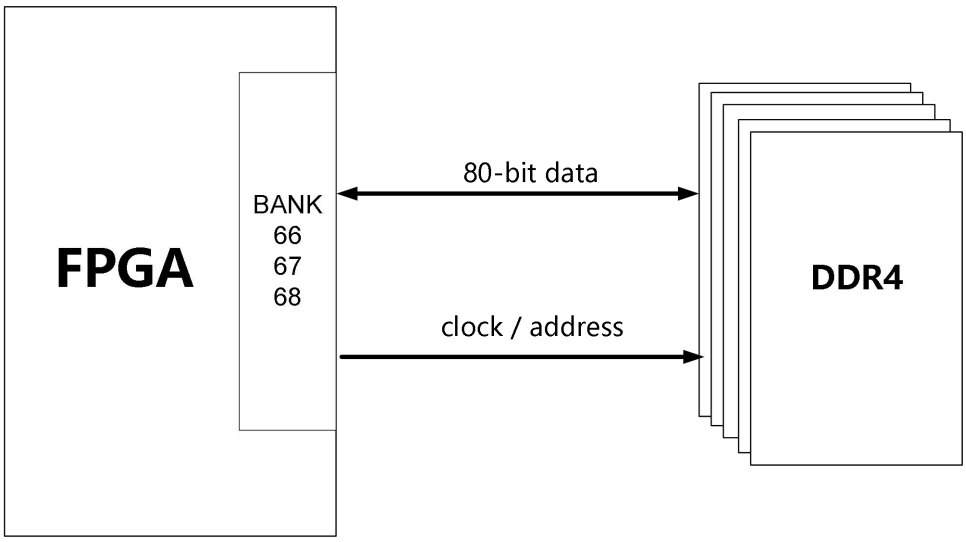


Figure 2.3.1 - Partial Schematic Diagram of DDR4 DRAM

DDR4 SDRAM pin assignment:

Signal name	FPGA pin names	FPGA pin numbers
DDR4_D0	IO_L20P_T3L_N2_AD1P_66	AJ28
DDR4_D1	IO_L24P_T3U_N10_66	AK27
DDR4_D2	IO_L21N_T3L_N5_AD8N_66	AK26
DDR4_D3	IO_L24N_T3U_N11_66	AL27
DDR4_D4	IO_L21P_T3L_N4_AD8P_66	AJ26

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Signal name	FPGA pin names	FPGA pin numbers
DDR4_D5	IO_L23P_T3U_N8_66	AN26
DDR4_D6	IO_L23N_T3U_N9_66	AN27
DDR4_D7	IO_L20N_T3L_N3_AD1N_66	AK28
DDR4_D8	IO_L15P_T2L_N4_AD11P_66	AK22
DDR4_D9	IO_L14P_T2L_N2_GC_66	AL24
DDR4_D10	IO_L17N_T2U_N9_AD10N_66	AJ23
DDR4_D11	IO_L14N_T2L_N3_GC_66	AM25
DDR4_D12	IO_L17P_T2U_N8_AD10P_66	AH23
DDR4_D13	IO_L18N_T2U_N11_AD2N_66	AK24
DDR4_D14	IO_L15N_T2L_N5_AD11N_66	AK23
DDR4_D15	IO_L18P_T2U_N10_AD2P_66	AJ24
DDR4_D16	IO_L12P_T1U_N10_GC_66	AN25
DDR4_D17	IO_L9N_T1L_N5_AD12N_66	AP23
DDR4_D18	IO_L11P_T1U_N8_GC_66	AP24
DDR4_D19	IO_L8P_T1L_N2_AD5P_66	AT25
DDR4_D20	IO_L9P_T1L_N4_AD12P_66	AN23
DDR4_D21	IO_L12N_T1U_N11_GC_66	AP26
DDR4_D22	IO_L11N_T1U_N9_GC_66	AP25
DDR4_D23	IO_L8N_T1L_N3_AD5N_66	AT26
DDR4_D24	IO_L3P_T0L_N4_AD15P_66	AU23
DDR4_D25	IO_L6P_T0U_N10_AD6P_66	AV26
DDR4_D26	IO_L5N_T0U_N9_AD14N_66	AU24
DDR4_D27	IO_L2P_T0L_N2_66	AW25
DDR4_D28	IO_L5P_T0U_N8_AD14P_66	AT24
DDR4_D29	IO_L2N_T0L_N3_66	AW26
DDR4_D30	IO_L3N_T0L_N5_AD15N_66	AV23
DDR4_D31	IO_L6N_T0U_N11_AD6N_66	AV27
DDR4_D32	IO_L21P_T3L_N4_AD8P_68	AM38

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Signal name	FPGA pin names	FPGA pin numbers
DDR4_D33	IO_L24N_T3U_N11_68	AK39
DDR4_D34	IO_L23N_T3U_N9_68	AL37
DDR4_D35	IO_L20P_T3L_N2_AD1P_68	AL39
DDR4_D36	IO_L21N_T3L_N5_AD8N_68	AN38
DDR4_D37	IO_L24P_T3U_N10_68	AJ39
DDR4_D38	IO_L23P_T3U_N8_68	AL36
DDR4_D39	IO_L20N_T3L_N3_AD1N_68	AM39
DDR4_D40	IO_L18N_T2U_N11_AD2N_68	AM35
DDR4_D41	IO_L18P_T2U_N10_AD2P_68	AL35
DDR4_D42	IO_L14N_T2L_N3_GC_68	AM34
DDR4_D43	IO_L14P_T2L_N2_GC_68	AL34
DDR4_D44	IO_L17P_T2U_N8_AD10P_68	AH33
DDR4_D45	IO_L15N_T2L_N5_AD11N_68	AK35
DDR4_D46	IO_L17N_T2U_N9_AD10N_68	AJ33
DDR4_D47	IO_L15P_T2L_N4_AD11P_68	AJ34
DDR4_D48	IO_L11P_T1U_N8_GC_68	AK32
DDR4_D49	IO_L11N_T1U_N9_GC_68	AL32
DDR4_D50	IO_L8N_T1L_N3_AD5N_68	AJ30
DDR4_D51	IO_L12N_T1U_N11_GC_68	AM33
DDR4_D52	IO_L9P_T1L_N4_AD12P_68	AH31
DDR4_D53	IO_L9N_T1L_N5_AD12N_68	AH32
DDR4_D54	IO_L8P_T1L_N2_AD5P_68	AJ29
DDR4_D55	IO_L12P_T1U_N10_GC_68	AM32
DDR4_D56	IO_L5P_T0U_N8_AD14P_68	AL29
DDR4_D57	IO_L2N_T0L_N3_68	AM30
DDR4_D58	IO_L5N_T0U_N9_AD14N_68	AM29
DDR4_D59	IO_L6N_T0U_N11_AD6N_68	AN33
DDR4_D60	IO_L3P_T0L_N4_AD15P_68	AP28

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Signal name	FPGA pin names	FPGA pin numbers
DDR4_D61	IO_L2P_T0L_N2_68	AL30
DDR4_D62	IO_L3N_T0L_N5_AD15N_68	AP29
DDR4_D63	IO_L6P_T0U_N10_AD6P_68	AN32
DDR4_D64	IO_L5N_T0U_N9_AD14N_67	AU29
DDR4_D65	IO_L6N_T0U_N11_AD6N_67	AW31
DDR4_D66	IO_L3P_T0L_N4_AD15P_67	AW28
DDR4_D67	IO_L6P_T0U_N10_AD6P_67	AV31
DDR4_D68	IO_L5P_T0U_N8_AD14P_67	AT29
DDR4_D69	IO_L2N_T0L_N3_67	AU30
DDR4_D70	IO_L3N_T0L_N5_AD15N_67	AW29
DDR4_D71	IO_L2P_T0L_N2_67	AT30
DDR4_D72	IO_L9P_T1L_N4_AD12P_67	AT35
DDR4_D73	IO_L8P_T1L_N2_AD5P_67	AW34
DDR4_D74	IO_L11N_T1U_N9_GC_67	AU33
DDR4_D75	IO_L12P_T1U_N10_GC_67	AU34
DDR4_D76	IO_L11P_T1U_N8_GC_67	AU32
DDR4_D77	IO_L9N_T1L_N5_AD12N_67	AT36
DDR4_D78	IO_L12N_T1U_N11_GC_67	AU35
DDR4_D79	IO_L8N_T1L_N3_AD5N_67	AW35
DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_66	AL25
DDR4_DM1	IO_L13P_T2L_N0_GC_QBC_66	AM23
DDR4_DM2	IO_L7P_T1L_N0_QBC_AD13P_66	AR23
DDR4_DM3	IO_L1P_T0L_N0_DBC_66	AW23
DDR4_DM4	IO_L19P_T3L_N0_DBC_AD9P_68	AM37
DDR4_DM5	IO_L13P_T2L_N0_GC_QBC_68	AK33
DDR4_DM6	IO_L7P_T1L_N0_QBC_AD13P_68	AH30
DDR4_DM7	IO_L1P_T0L_N0_DBC_68	AM28
DDR4_DM8	IO_L1P_T0L_N0_DBC_67	AU28

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Signal name	FPGA pin names	FPGA pin numbers
DDR4_DM9	IO_L7P_T1L_N0_QBC_AD13P_67	AV35
DDR4_DQS0_N	IO_L22N_T3U_N7_DBC_AD0N_66	AH27
DDR4_DQS0_P	IO_L22P_T3U_N6_DBC_AD0P_66	AH26
DDR4_DQS1_N	IO_L16N_T2U_N7_QBC_AD3N_66	AJ25
DDR4_DQS1_P	IO_L16P_T2U_N6_QBC_AD3P_66	AH25
DDR4_DQS2_N	IO_L10N_T1U_N7_QBC_AD4N_66	AR27
DDR4_DQS2_P	IO_L10P_T1U_N6_QBC_AD4P_66	AR26
DDR4_DQS3_N	IO_L4N_T0U_N7_DBC_AD7N_66	AV25
DDR4_DQS3_P	IO_L4P_T0U_N6_DBC_AD7P_66	AU25
DDR4_DQS4_N	IO_L22N_T3U_N7_DBC_AD0N_68	AK38
DDR4_DQS4_P	IO_L22P_T3U_N6_DBC_AD0P_68	AK37
DDR4_DQS5_N	IO_L16N_T2U_N7_QBC_AD3N_68	AN36
DDR4_DQS5_P	IO_L16P_T2U_N6_QBC_AD3P_68	AN35
DDR4_DQS6_N	IO_L10N_T1U_N7_QBC_AD4N_68	AL31
DDR4_DQS6_P	IO_L10P_T1U_N6_QBC_AD4P_68	AK31
DDR4_DQS7_N	IO_L4N_T0U_N7_DBC_AD7N_68	AN31
DDR4_DQS7_P	IO_L4P_T0U_N6_DBC_AD7P_68	AN30
DDR4_DQS8_N	IO_L4N_T0U_N7_DBC_AD7N_67	AW30
DDR4_DQS8_P	IO_L4P_T0U_N6_DBC_AD7P_67	AV30
DDR4_DQS9_N	IO_L10N_T1U_N7_QBC_AD4N_67	AV33
DDR4_DQS9_P	IO_L10P_T1U_N6_QBC_AD4P_67	AV32
DDR4_OTD	IO_L17N_T2U_N9_AD10N_67	AR33
DDR4_PAR	IO_L7N_T1L_N1_QBC_AD13N_67	AV36
DDR4_RAS_B	IO_L16N_T2U_N7_QBC_AD3N_67	AP35
DDR4_RST	IO_T2U_N12_68	AH34
DDR4_WE_B	IO_T2U_N12_67	AP31
DDR4_A0	IO_L22N_T3U_N7_DBC_AD0N_67	AV38
DDR4_A1	IO_L21P_T3L_N4_AD8P_67	AR38

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Signal name	FPGA pin names	FPGA pin numbers
DDR4_A2	IO_L20N_T3L_N3_AD1N_67	AV37
DDR4_A3	IO_L18N_T2U_N11_AD2N_67	AR36
DDR4_A4	IO_L24N_T3U_N11_67	AU39
DDR4_A5	IO_L23P_T3U_N8_67	AP38
DDR4_A6	IO_L15N_T2L_N5_AD11N_67	AT31
DDR4_A7	IO_L23N_T3U_N9_67	AP39
DDR4_A8	IO_L1N_T0L_N1_DBC_67	AV28
DDR4_A9	IO_L24P_T3U_N10_67	AT39
DDR4_A10	IO_L22P_T3U_N6_DBC_AD0P_67	AU38
DDR4_A11	IO_T3U_N12_67	AW36
DDR4_A12	IO_L19P_T3L_N0_DBC_AD9P_67	AR37
DDR4_A13	IO_L21N_T3L_N5_AD8N_67	AR39
DDR4_ACT_B	IO_L19N_T3L_N1_DBC_AD9N_67	AT37
DDR4_ALERT_B	IO_L13N_T2L_N1_GC_QBC_68	AK34
DDR4_BA0	IO_T1U_N12_67	AW33
DDR4_BA1	IO_L18P_T2U_N10_AD2P_67	AP36
DDR4_BG0	IO_L15P_T2L_N4_AD11P_67	AR31
DDR4_CAS_B	IO_L16P_T2U_N6_QBC_AD3P_67	AP34
DDR4_CKE	IO_L20P_T3L_N2_AD1P_67	AU37
DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_67	AT34
DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_67	AR34
DDR4_CLKREF_N	IO_L14N_T2L_N3_GC_67	AT32
DDR4_CLKREF_P	IO_L14P_T2L_N2_GC_67	AR32
DDR4_CS_B	IO_L17P_T2U_N8_AD10P_67	AP33

Table 2.3.2 - DDR4 SDRAM Pin Assignment

2.4 QSPI Flash

The SoM is equipped with two 64MB Quad -SPI FLASH chips, model MT25QU512ABB1EW9, which use the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can

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store the FPGA configuration binary file and other user data files. The specific model and related parameters of the QSPI FLASH are shown in the table .

Position	Chip type	Capacity	Factory
U10 , U11	MT25QU512ABB1EW9	512 Mbit	Micron

Table 2.4.1 - QSPI Flash Models and Parameters

The QSPI FLASH module is connected to dedicated pins on the FPGA chip, with its clock pin linked to CLK0 on Bank 0 and data pins connected to both Bank 0 and Bank 65. The diagram below illustrates the connection between the QSPI Flash and the FPGA chip.

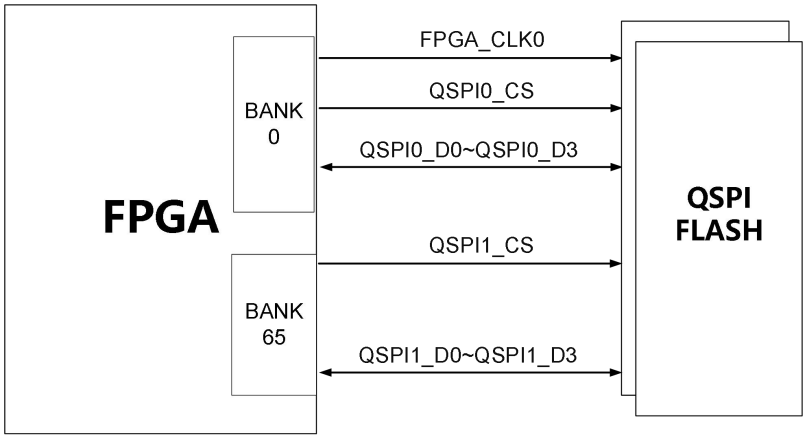


Figure 2.4.1 - QSPI Flash Connection Diagram

Configure chip pin assignments:

Signal name	FPGA pin names	FPGA pin numbers
QSPI_CLK	CCLK_0	AD23
QSPI0_CS	RDWR_FCS_B_0	AG22
QSPI0_DQ0	D00_MOSI_0	AD25
QSPI0_DQ1	D01_DIN_0	AD26
QSPI0_DQ2	D02_0	AE22
QSPI0_DQ3	D03_0	AE23
QSPI1_CS	IO_L2N_T0L_N3_FWE_FCS2_B_65	AV11
QSPI1_DQ0	IO_L22P_T3U_N6_DBC_AD0P_D04_65	AM12
QSPI1_DQ1	IO_L22N_T3U_N7_DBC_AD0N_D05_65	AN12
QSPI1_DQ2	IO_L21P_T3L_N4_AD8P_D06_65	AR13
QSPI1_DQ3	IO_L21N_T3L_N5_AD8N_D07_65	AR12

Table 2.4.2 - QSPI Pin Assignment

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2.5 Clock Configuration

The SoM provides two 200 MHz differential active clocks for the FPGA system. These provide differential clock sources for the FPGA logic sections. A schematic diagram of the clock circuit design is shown in Figure 2.5.1 below .

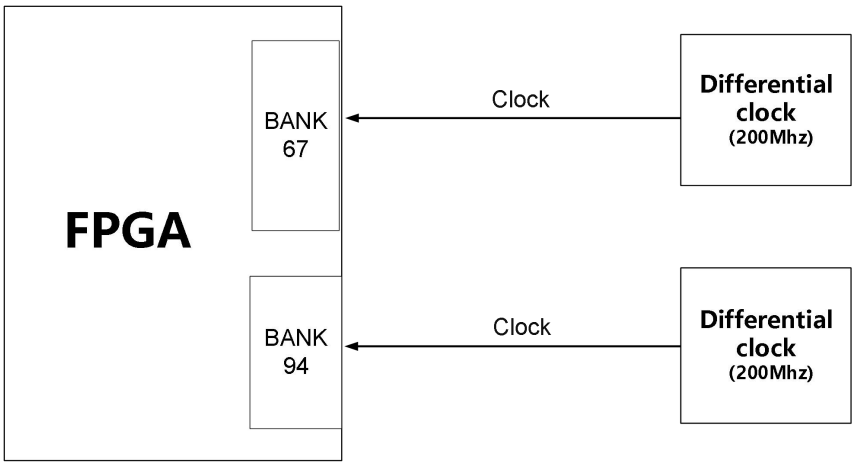


Figure 2.5.1 - SoM clock source

FPGA system clock source

The som provides two 200MHz differential crystal oscillators to provide reference clocks for the DDR4 controller and FPGA logic . The crystal oscillator outputs are connected to the global clocks of FPGAs BANK 66 and BANK 94. This global clock can be used to drive the DDR4 controller and user logic circuits within the FPGA . The FPGA pin assignments for this clock source are shown in the table below:

Signal name	FPGA pin names	FPGA pins
B94_L5_P	IO_L5P_HDGC_94	G12
B94_L5_N	IO_L5N_HDGC_94	G11
DDR4_CLKREF_P	IO_L14P_T2L_N2_GC_67	AR32
DDR4_CLKREF_N	IO_L14N_T2L_N3_GC_67	AT32

Table 2.5.1 - Clock Pin Assignment

2.6 LED

The ACKU15S SoM has three red LEDs: one is a power indicator (PWR1) , one is configuration LED (D1) , and one is user indicator (LED1). The indicator lights up when the som is powered on; the configuration LED lights up after the FPGA configuration program is completed. The user indicator can be used to customize function indications. A schematic diagram of the LED hardware connection is shown in Figure 2.6.1 .

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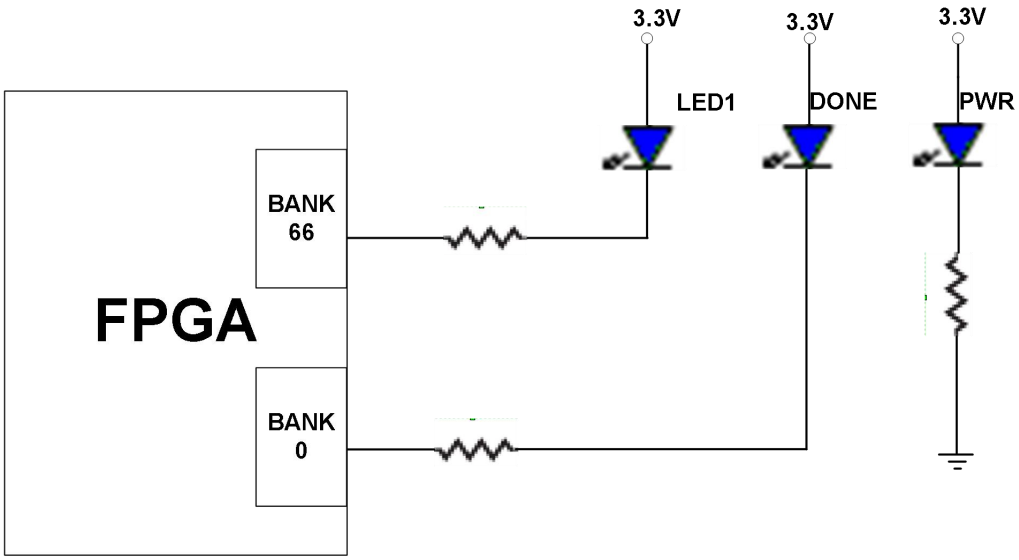


Figure 2.6.1 - Hardware connection diagram of LED lights on the SoM

User indicator light pin assignment:

Signal name	FPGA pin names	FPGA pins
LED1	IO_T1U_N12_66	AT27

Table 2.6.1 - User Indicator Pin Assignment

2.7 Power Supply

The ACKU15S SoM operates on a + 12V power supply , connected to the carrier board. The + 12V power supply is generated by the IS6608 DC-DC power chip , providing up to 60A of output current to meet the core voltage's current requirements. This + 12V power then powers the FPGA auxiliary power supply and high-speed transceiver via three DC-DC chips : SGM61163 (VCCAUX) , IS66066 (MGTAVCC) , and MGTAVTT . Simultaneously, the + 12V power supply, through the ETA1471 and SGM61163 DC-DC chips, generates +1.2V (VCC1V8_FPGA) and D3V3 power supplies to the DDR4, FPGA bank, and peripherals . Additionally, the D3V3 power supply , through two ETA5060 LDO chips, generates +1.8V for the high-speed transceiver and the FPGA's ADC . The VTT for DDR4 and the DDR2V5 voltage are generated by the TPS51200 and ETA5050 .

Because FPGA power supplies have specific power-on sequence requirements, we have designed the circuit according to the chip's power requirements to ensure normal chip operation. The power supply design diagram on the board is shown in Figure 2.7.1 below :

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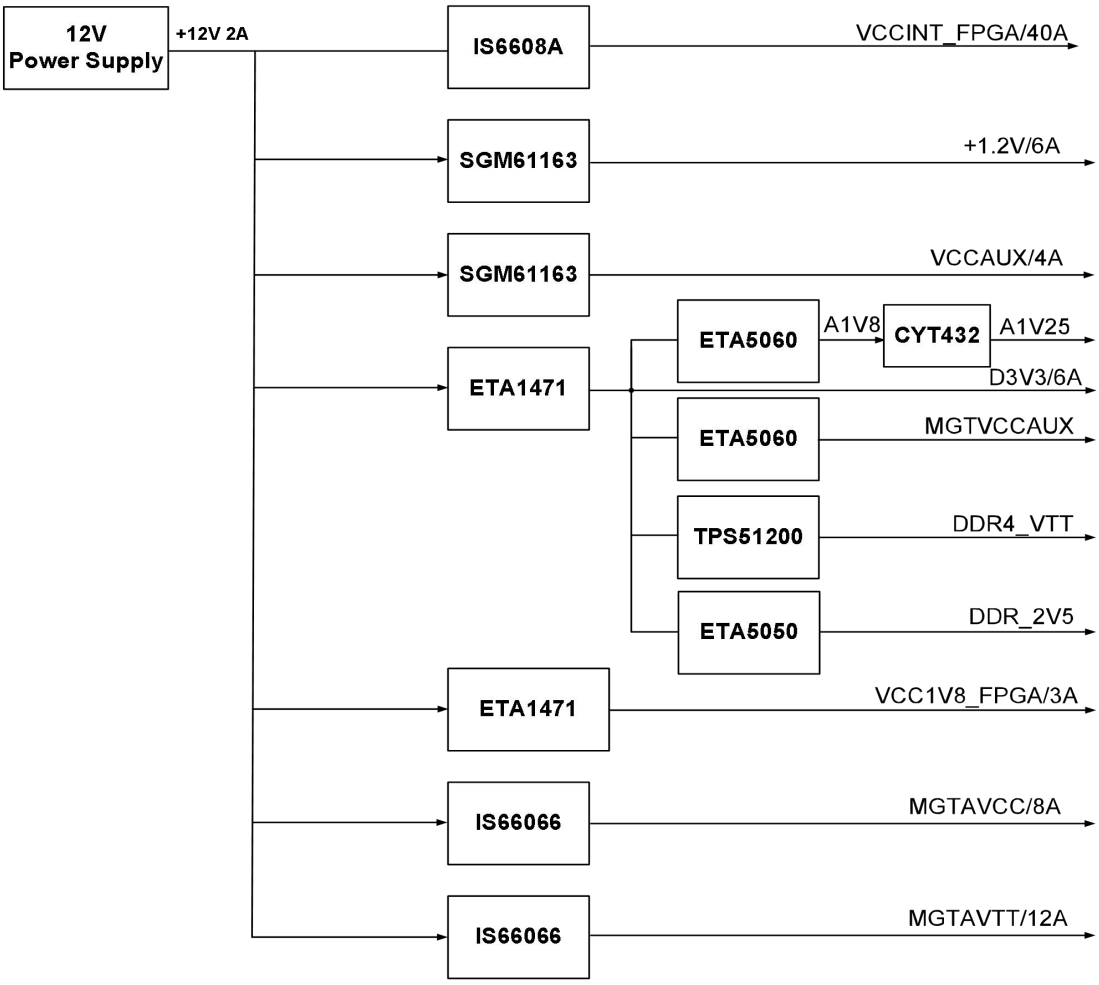


Figure 2.7.1 - Power interface section in the schematic diagram

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2.8 Structural Diagram

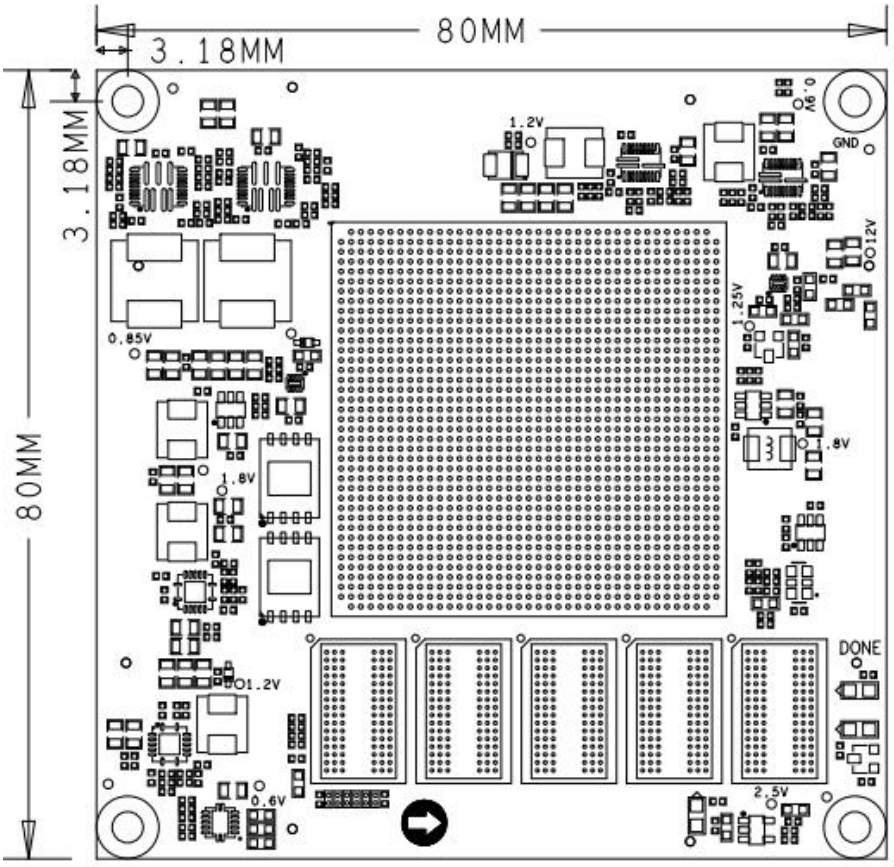


Figure 2.8.1 - Top View of the SoM

2.9 Connector Pin Definitions

The SoM has four high-speed expansion ports, connected to the carrier board via four 240- pin board to board connectors (J1 ~ J4) . Power to the SoM is input via connector J3. J2 connects to the carrier board's adjustable voltages VCCIO_64 and VCCIO_65, J3 connects to the carrier board's +12V power supply, and J4 connects to the carrier board's VCCO_90_91_93_94. The adjustable voltage can be selected by replacing the LDO chip on the carrier board or by using a 0Ω resistor.

J1 Connector Pin Assignment

J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
A1	B90_L10_N	B4	B1	B90_L12_N	A6
A2	B90_L10_P	B5	B2	B90_L12_P	B6
A3	B90_L8_N	C4	B3	B90_L11_N	A3
A4	B90_L8_P	C5	B4	B90_L11_P	A4

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J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
A5	GND	-	B5	GND	-
A6	B90_L9_N	B2	B6	B90_L7_N	C3
A7	B90_L9_P	C2	B7	B90_L7_P	D3
A8	B90_L4_N	E1	B8	B90_L6_N	D1
A9	B90_L4_P	F1	B9	B90_L6_P	D2
A10	GND	-	B10	GND	-
A11	B90_L5_N	D5	B11	B90_L3_N	F2
A12	B90_L5_P	D6	B12	B90_L3_P	F3
A13	B90_L1_N	E4	B13	B90_L2_N	E3
A14	B90_L1_P	E5	B14	B90_L2_P	F4
A15	GND	-	B15	GND	-
A16	B91_L11_N	A9	B16	B91_L9_N	A7
A17	B91_L11_P	B10	B17	B91_L9_P	B7
A18	B91_L12_N	A11	B18	B91_L10_N	A8
A19	B91_L12_P	B11	B19	B91_L10_P	B9
A20	GND	-	B20	GND	-
A21	B91_L7_N	C7	B21	B91_L5_N	D7
A22	B91_L7_P	C8	B22	B91_L5_P	D8
A23	B91_L3_N	E8	B23	B91_L1_N	E6
A24	B91_L3_P	F9	B24	B91_L1_P	F6
A25	GND	-	B25	GND	-
A26	B91_L8_N	C9	B26	B91_L2_N	F7
A27	B91_L8_P	C10	B27	B91_L2_P	F8
A28	B91_L6_N	D10	B28	B91_L4_N	E9
A29	B91_L6_P	D11	B29	B91_L4_P	E10
A30	GND	-	B30	GND	-
A31	B93_L12_N	K10	B31	B93_L10_N	K13

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J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
A32	B93_L12_P	K11	B32	B93_L10_P	L13
A33	B93_L7_N	L14	B33	B93_L11_N	L11
A34	B93_L7_P	M14	B34	B93_L11_P	L12
A35	GND	-	B35	GND	-
A36	B93_L9_N	M10	B36	B93_L8_N	M11
A37	B93_L9_P	N10	B37	B93_L8_P	M12
A38	B93_L3_N	P12	B38	B93_L4_N	P10
A39	B93_L3_P	P13	B39	B93_L4_P	P11
A40	GND	-	B40	GND	-
A41	B93_L6_N	N12	B41	B93_L2_N	R13
A42	B93_L6_P	N13	B42	B93_L2_P	R14
A43	B93_L5_N	N14	B43	B93_L1_N	P15
A44	B93_L5_P	N15	B44	B93_L1_P	R15
A45	GND	-	B45	GND	-
A46	GND	-	B46	GND	-
A47	MGT227_CLK0_P	AE12	B47	MGT227_CLK1_P	AD10
A48	MGT227_CLK0_N	AE11	B48	MGT227_CLK1_N	AD9
A49	GND	-	B49	GND	-
A50	MGT227_RX3_P	AD2	B50	MGT227_TX3_P	AD6
A51	MGT227_RX3_N	AD1	B51	MGT227_TX3_N	AD5
A52	GND	-	B52	GND	-
A53	MGT227_RX2_P	AE4	B53	MGT227_TX2_P	AE8
A54	MGT227_RX2_N	AE3	B54	MGT227_TX2_N	AE7
A55	GND	-	B55	GND	-
A56	MGT227_RX1_P	AF2	B56	MGT227_TX1_P	AF6
A57	MGT227_RX1_N	AF1	B57	MGT227_TX1_N	AF5
A58	GND	-	B58	GND	-

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J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
A59	MGT227_RX0_P	AG4	B59	MGT227_TX0_P	AG8
A60	MGT227_RX0_N	AG3	B60	MGT227_TX0_N	AG7

Table 2.9.1 - J1 Connector Pin Assignment

J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
C1	MGT231_CLK0_P	U12	D1	MGT231_CLK1_P	T10
C2	MGT231_CLK0_N	U11	D2	MGT231_CLK1_N	T9
C3	GND	-	D3	GND	-
C4	MGT231_RX3_P	H2	D4	MGT231_TX3_P	H6
C5	MGT231_RX3_N	H1	D5	MGT231_TX3_N	H5
C6	GND	-	D6	GND	-
C7	MGT231_RX2_P	J4	D7	MGT231_TX2_P	J8
C8	MGT231_RX2_N	J3	D8	MGT231_TX2_N	J7
C9	GND	-	D9	GND	-
C10	MGT231_RX1_P	K2	D10	MGT231_TX1_P	K6
C11	MGT231_RX1_N	K1	D11	MGT231_TX1_N	K5
C12	GND	-	D12	GND	-
C13	MGT231_RX0_P	L4	D13	MGT231_TX0_P	L8
C14	MGT231_RX0_N	L3	D14	MGT231_TX0_N	L7
C15	GND	-	D15	GND	-
C16	MGT230_RX3_P	M2	D16	MGT230_TX3_P	M6
C17	MGT230_RX3_N	M1	D17	MGT230_TX3_N	M5
C18	GND	-	D18	GND	-
C19	MGT230_RX2_P	N4	D19	MGT230_TX2_P	N8
C20	MGT230_RX2_N	N3	D20	MGT230_TX2_N	N7
C21	GND	-	D21	GND	-
C22	MGT230_RX1_P	P2	D22	MGT230_TX1_P	P6

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J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
C23	MGT230_RX1_N	P1	D23	MGT230_TX1_N	P5
C24	GND	-	D24	GND	-
C25	MGT230_RX0_P	R4	D25	MGT230_TX0_P	R8
C26	MGT230_RX0_N	R3	D26	MGT230_TX0_N	R7
C27	GND	-	D27	GND	-
C28	MGT230_CLK1_P	V10	D28	MGT230_CLK0_P	W12
C29	MGT230_CLK1_N	V9	D29	MGT230_CLK0_N	W11
C30	GND	-	D30	GND	-
C31	MGT229_RX3_P	T2	D31	MGT229_TX3_P	T6
C32	MGT229_RX3_N	T1	D32	MGT229_TX3_N	T5
C33	GND	-	D33	GND	-
C34	MGT229_RX2_P	U4	D34	MGT229_TX2_P	U8
C35	MGT229_RX2_N	U3	D35	MGT229_TX2_N	U7
C36	GND	-	D36	GND	-
C37	MGT229_RX1_P	V2	D37	MGT229_TX1_P	V6
C38	MGT229_RX1_N	V1	D38	MGT229_TX1_N	V5
C39	GND	-	D39	GND	-
C40	MGT229_RX0_P	W4	D40	MGT229_TX0_P	W8
C41	MGT229_RX0_N	W3	D41	MGT229_TX0_N	W7
C42	GND	-	D42	GND	-
C43	MGT229_CLK1_P	Y10	D43	MGT229_CLK0_P	AA12
C44	MGT229_CLK1_N	Y9	D44	MGT229_CLK0_N	AA11
C45	GND	-	D45	GND	-
C46	GND	-	D46	GND	-
C47	MGT228_RX3_P	Y2	D47	MGT228_TX3_P	Y6
C48	MGT228_RX3_N	Y1	D48	MGT228_TX3_N	Y5
C49	GND	-	D49	GND	-

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J1 pin	Signal name	Pin number	J1 pin	Signal name	Pin number
C50	MGT228_RX2_P	AA4	D50	MGT228_TX2_P	AA8
C51	MGT228_RX2_N	AA3	D51	MGT228_TX2_N	AA7
C52	GND	-	D52	GND	-
C53	MGT228_RX1_P	AB2	D53	MGT228_TX1_P	AB6
C54	MGT228_RX1_N	AB1	D54	MGT228_TX1_N	AB5
C55	GND	-	D55	GND	-
C56	MGT228_RX0_P	AC4	D56	MGT228_TX0_P	AC8
C57	MGT228_RX0_N	AC3	D57	MGT228_TX0_N	AC7
C58	GND	-	D58	GND	-
C59	MGT228_CLK0_P	AC12	D59	MGT228_CLK1_P	AB10
C60	MGT228_CLK0_N	AC11	D60	MGT228_CLK1_N	AB9

Table 2.9.2 - J1 Connector Pin Assignment

J2 connector

J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
A1	FPGA_VP_IN	W20	B1	FPGA_TDI	AG24
A2	FPGA_VN_IN	Y19	B2	FPGA_TDO	AG27
A3	GND	-	B3	GND	-
A4	B64_L1_P	AU22	B4	B64_L19_P	AH21
A5	B64_L1_N	AV22	B5	B64_L19_N	AJ21
A6	GND	-	B6	GND	-
A7	B64_L21_P	AJ20	B7	B64_L10_P	AK21
A8	B64_L21_N	AJ19	B8	B64_L10_N	AL21
A9	GND	-	B9	GND	-
A10	B64_L8_P	AL22	B10	B65_L17_P	AJ16
A11	B64_L8_N	AM22	B11	B65_L17_N	AJ15
A12	GND	-	B12	GND	-
A13	B65_L18_P	AK16	B13	B65_L16_P	AK17

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J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
A14	B65_L18_N	AL16	B14	B65_L16_N	AL17
A15	GND	-	B15	GND	-
A16	B65_L20_P	AN13	B16	B65_L14_P	AM15
A17	B65_L20_N	AP13	B17	B65_L14_N	AN15
A18	GND	-	B18	GND	-
A19	B65_L11_P	AR14	B19	B65_L10_P	AP16
A20	B65_L11_N	AT14	B20	B65_L10_N	AR16
A21	GND	-	B21	GND	-
A22	B65_L7_P	AV16	B22	B65_L8_P	AT15
A23	B65_L7_N	AW16	B23	B65_L8_N	AU15
A24	GND	-	B24	GND	-
A25	B65_L9_P	AV15	B25	B65_L6_P	AU14
A26	B65_L9_N	AW15	B26	B65_L6_N	AU13
A27	GND	-	B27	GND	-
A28	VCCIO_64	AK20, AN19, AT8	B28	B65_T2U	AN16
A29	VCCIO_65	AK15, AN14, AT13	B29	B65_T3U	AP10
A30	GND	-	B30	GND	-
A31	B65_L5_P	AV13	B31	B65_L3_P	AW14
A32	B65_L5_N	AV12	B32	B65_L3_N	AW13
A33	GND	-	B33	GND	-
A34	B65_L12_P	AP15	B34	B65_L24_P	AM14
A35	B65_L12_N	AP14	B35	B65_L24_N	AM13
A36	GND	-	B36	GND	-
A37	B65_L13_P	AL15	B37	B65_L15_P	AJ14
A38	B65_L13_N	AL14	B38	B65_L15_N	AK14
A39	GND	-	B39	GND	-
A40	B65_L1_P	AW11	B40	B65_L4_P	AU10

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J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
A41	B65_L1_N	AW10	B41	B65_L4_N	AV10
A42	GND	-	B42	GND	-
A43	B65_L19_P	AT12	B43	B65_L23_P	AP11
A44	B65_L19_N	AT11	B44	B65_L23_N	AR11
A45	GND	-	B45	GND	-
A46	GND	-	B46	GND	-
A47	MGT225_RX0_P	AR4	B47	MGT225_TX0_P	AR8
A48	MGT225_RX0_N	AR3	B48	MGT225_TX0_N	AR7
A49	GND	-	B49	GND	-
A50	MGT225_RX1_P	AP2	B50	MGT225_TX1_P	AP6
A51	MGT225_RX1_N	AP1	B51	MGT225_TX1_N	AP5
A52	GND	-	B52	GND	-
A53	MGT225_RX2_P	AN4	B53	MGT225_TX2_P	AN8
A54	MGT225_RX2_N	AN3	B54	MGT225_TX2_N	AN7
A55	GND	-	B55	GND	-
A56	MGT225_RX3_P	AM2	B56	MGT225_TX3_P	AM6
A57	MGT225_RX3_N	AM1	B57	MGT225_TX3_N	AM5
A58	GND	-	B58	GND	-
A59	MGT225_CLK0_P	AJ12	B59	MGT225_CLK1_P	AH10
A60	MGT225_CLK0_N	AJ11	B60	MGT225_CLK1_N	AH9

Table 2.9.3 - J2 Connector Pin Assignment

J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
C1	FPGA_TMS	AD22	D1	B64_L9_P	AP21
C2	FPGA_TCK	AG23	D2	B64_L9_N	AP20
C3	GND	-	D3	GND	-
C4	B64_L5_P	AT22	D4	B64_L7_P	AR22

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J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
C5	B64_L5_N	AT21	D5	B64_L7_N	AR21
C6	GND	-	D6	GND	-
C7	B64_L3_P	AV21	D7	B64_L15_P	AT20
C8	B64_L3_N	AW21	D8	B64_L15_N	AT19
C9	GND	-	D9	GND	-
C10	B64_L12_P	AL20	D10	B64_L2_P	AU20
C11	B64_L12_N	AM20	D11	B64_L2_N	AV20
C12	GND	-	D12	GND	-
C13	B64_L11_P	AN21	D13	B64_L17_P	AU19
C14	B64_L11_N	AN20	D14	B64_L17_N	AU18
C15	GND	-	D15	GND	-
C16	B64_L20_P	AL19	D16	B64_L4_P	AW20
C17	B64_L20_N	AM19	D17	B64_L4_N	AW19
C18	GND	-	D18	GND	-
C19	B64_L13_P	AP19	D19	B64_L6_P	AV18
C20	B64_L13_N	AR19	D20	B64_L6_N	AW18
C21	GND	-	D21	GND	-
C22	B64_L14_P	AN18	D22	B64_L16_P	AT17
C23	B64_L14_N	AP18	D23	B64_L16_N	AU17
C24	GND	-	D24	GND	-
C25	B64_L24_P	AM18	D25	B64_L18_P	AR18
C26	B64_L24_N	AM17	D26	B64_L18_N	AR17
C27	GND	-	D27	GND	-
C28	B64_L22_P	AK19	D28	B64_L23_P	AH18
C29	B64_L22_N	AK18	D29	B64_L23_N	AJ18
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-

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J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
C32	MGT224_CLK0_P	AM10	D32	MGT224_CLK1_P	AK10
C33	MGT224_CLK0_N	AM9	D33	MGT224_CLK1_N	AK9
C34	GND	-	D34	GND	-
C35	MGT224_RX3_P	AT2	D35	MGT224_TX3_P	AT6
C36	MGT224_RX3_N	AT1	D36	MGT224_TX3_N	AT5
C37	GND	-	D37	GND	-
C38	MGT224_RX2_P	AU4	D38	MGT224_TX2_P	AU8
C39	MGT224_RX2_N	AU3	D39	MGT224_TX2_N	AU7
C40	GND	-	D40	GND	-
C41	MGT224_RX0_P	AW4	D41	MGT224_TX0_P	AW8
C42	MGT224_RX0_N	AW3	D42	MGT224_TX0_N	AW7
C43	GND	-	D43	GND	-
C44	MGT224_RX1_P	AV2	D44	MGT224_TX1_P	AV6
C45	MGT224_RX1_N	AV1	D45	MGT224_TX1_N	AV5
C46	GND	-	D46	GND	-
C47	MGT226_CLK0_P	AG12	D47	MGT226_CLK1_P	AF10
C48	MGT226_CLK0_N	AG11	D48	MGT226_CLK1_N	AF9
C49	GND	-	D49	GND	-
C50	MGT226_RX0_P	AL4	D50	MGT226_TX0_P	AL8
C51	MGT226_RX0_N	AL3	D51	MGT226_TX0_N	AL7
C52	GND	-	D52	GND	-
C53	MGT226_RX1_P	AK2	D53	MGT226_TX1_P	AK6
C54	MGT226_RX1_N	AK1	D54	MGT226_TX1_N	AK5
C55	GND	-	D55	GND	-
C56	MGT226_RX2_P	AJ4	D56	MGT226_TX2_P	AJ8
C57	MGT226_RX2_N	AJ3	D57	MGT226_TX2_N	AJ7
C58	GND	-	D58	GND	-

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J2 pin	Signal name	Pin number	J2 pin	Signal name	Pin number
C59	MGT226_RX3_P	AH2	D59	MGT226_TX3_P	AH6
C60	MGT226_RX3_N	AH1	D60	MGT226_TX3_N	AH5

Table 2.9.4 - J2 Connector Pin Assignment

J3 connector pin assignment

J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
A1	+12V	-	B1	+12V	-
A2	+12V	-	B2	+12V	-
A3	GND	-	B3	GND	-
A4	FMC1_VREF_A_M2C_1	M27	B4	VCCIO_71	B18、E17、H16
A5	VCCAUX_PG	-	B5	FMC1_VREF_A_M2C_2	M24
A6	GND	-	B6	GND	-
A7	MGT131_RX3_P	J38	B7	MGT131_TX3_P	E33
A8	MGT131_RX3_N	J39	B8	MGT131_TX3_N	E34
A9	GND	-	B9	GND	-
A10	MGT131_RX2_P	K36	B10	MGT131_TX2_P	F35
A11	MGT131_RX2_N	K37	B11	MGT131_TX2_N	F36
A12	GND	-	B12	GND	-
A13	MGT131_RX1_P	L38	B13	MGT131_TX1_P	G33
A14	MGT131_RX1_N	L39	B14	MGT131_TX1_N	G34
A15	GND	-	B15	GND	-
A16	MGT131_RX0_P	M36	B16	MGT131_TX0_P	J33
A17	MGT131_RX0_N	M37	B17	MGT131_TX0_N	J34
A18	GND	-	B18	GND	-
A19	MGT131_CLK0_P	T27	B19	MGT131_CLK1_P	R29
A20	MGT131_CLK0_N	T28	B20	MGT131_CLK1_N	R30
A21	GND	-	B21	GND	-
A22	MGT129_RX3_P	U38	B22	MGT129_TX3_P	R33

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J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
A23	MGT129_RX3_N	U39	B23	MGT129_TX3_N	R34
A24	GND	-	B24	GND	-
A25	MGT129_RX2_P	V36	B25	MGT129_TX2_P	T31
A26	MGT129_RX2_N	V37	B26	MGT129_TX2_N	T32
A27	GND	-	B27	GND	-
A28	MGT129_RX1_P	W38	B28	MGT129_TX1_P	U33
A29	MGT129_RX1_N	W39	B29	MGT129_TX1_N	U34
A30	GND	-	B30	GND	-
A31	MGT129_RX0_P	Y36	B31	MGT129_TX0_P	V31
A32	MGT129_RX0_N	Y37	B32	MGT129_TX0_N	V32
A33	GND	-	B33	GND	-
A34	MGT129_CLK0_P	Y27	B34	MGT129_CLK1_P	W29
A35	MGT129_CLK0_N	Y28	B35	MGT129_CLK1_N	W30
A36	GND	-	B36	GND	-
A37	MGT127_CLK0_P	AE29	B37	MGT127_CLK1_P	AC29
A38	MGT127_CLK0_N	AE30	B38	MGT127_CLK1_N	AC30
A39	GND	-	B39	GND	-
A40	MGT127_RX3_P	AE38	B40	MGT127_TX3_P	AC33
A41	MGT127_RX3_N	AE39	B41	MGT127_TX3_N	AC34
A42	GND	-	B42	GND	-
A43	MGT127_RX2_P	AF36	B43	MGT127_TX2_P	AD31
A44	MGT127_RX2_N	AF37	B44	MGT127_TX2_N	AD32
A45	GND	-	B45	GND	-
A46	MGT127_RX1_P	AG38	B46	MGT127_TX1_P	AE33
A47	MGT127_RX1_N	AG39	B47	MGT127_TX1_N	AE34
A48	GND	-	B48	GND	-
A49	MGT127_RX0_P	AH36	B49	MGT127_TX0_P	AF31

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J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
A50	MGT127_RX0_N	AH37	B50	MGT127_TX0_N	AF32
A51	GND	-	B51	GND	-
A52	FMC2_VREF_A_M2C_1	AH20	B52	SELECTMAP_DATA6	AR13
A53	FMC2_VREF_A_M2C_2	AH16	B53	SELECTMAP_DATA7	AR12
A54	GND	-	B54	GND	-
A55	SELECTMAP_DATA0	AD25	B55	SELECTMAP_DATA3	AE23
A56	SELECTMAP_DATA1	AD26	B56	SELECTMAP_DATA5	AN12
A57	GND	-	B57	GND	-
A58	NC	-	B58	SELECTMAP_DATA4	AM12
A59	NC	-	B59	SELECTMAP_DATA2	AE22
A60	GND	-	B60	GND	-

Table 2.9.5 - J3 Connector Pin Assignment

J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
C1	+12V	-	D1	+12V	-
C2	+12V	-	D2	+12V	-
C3	GND	-	D3	GND	-
C4	VCCIO_70	B23、E22、H21	D4	VCCIO_69	B28、E27、H26
C5	FMC1_VREF_A_M2C_3	M17	D5	NC	-
C6	GND	-	D6	GND	-
C7	MGT132_RX3_P	C38	D7	MGT132_TX3_P	A33
C8	MGT132_RX3_N	C39	D8	MGT132_TX3_N	A34
C9	GND	-	D9	GND	-
C10	MGT132_RX2_P	E38	D10	MGT132_TX2_P	B35
C11	MGT132_RX2_N	E39	D11	MGT132_TX2_N	B36
C12	GND	-	D12	GND	-
C13	MGT132_RX1_P	G38	D13	MGT132_TX1_P	C33

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J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
C14	MGT132_RX1_N	G39	D14	MGT132_TX1_N	C34
C15	GND	-	D15	GND	-
C16	MGT132_RX0_P	H36	D16	MGT132_TX0_P	D35
C17	MGT132_RX0_N	H37	D17	MGT132_TX0_N	D36
C18	GND	-	D18	GND	-
C19	MGT132_CLK0_P	P27	D19	MGT132_CLK1_P	N29
C20	MGT132_CLK0_N	P28	D20	MGT132_CLK1_N	N30
C21	GND	-	D21	GND	-
C22	MGT130_RX3_P	N38	D22	MGT130_TX3_P	L33
C23	MGT130_RX3_N	N39	D23	MGT130_TX3_N	L34
C24	GND	-	D24	GND	-
C25	MGT130_RX2_P	P36	D25	MGT130_TX2_P	M31
C26	MGT130_RX2_N	P37	D26	MGT130_TX2_N	M32
C27	GND	-	D27	GND	-
C28	MGT130_RX1_P	R38	D28	MGT130_TX1_P	N33
C29	MGT130_RX1_N	R39	D29	MGT130_TX1_N	N34
C30	GND	-	D30	GND	-
C31	MGT130_RX0_P	T36	D31	MGT130_TX0_P	P31
C32	MGT130_RX0_N	T37	D32	MGT130_TX0_N	P32
C33	GND	-	D33	GND	-
C34	MGT130_CLK0_P	V27	D34	MGT130_CLK1_P	U29
C35	MGT130_CLK0_N	V28	D35	MGT130_CLK1_N	U30
C36	GND	-	D36	GND	-
C37	MGT128_CLK0_P	AB27	D37	MGT128_CLK1_P	AA29
C38	MGT128_CLK0_N	AB28	D38	MGT128_CLK1_N	AA30
C39	GND	-	D39	GND	-
C40	MGT128_RX3_P	AA38	D40	MGT128_TX3_P	W33

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J3 pin	Signal name	Pin number	J3 pin	Signal name	Pin number
C41	MGT128_RX3_N	AA39	D41	MGT128_TX3_N	W34
C42	GND	-	D42	GND	-
C43	MGT128_RX2_P	AB36	D43	MGT128_TX2_P	Y31
C44	MGT128_RX2_N	AB37	D44	MGT128_TX2_N	Y32
C45	GND	-	D45	GND	-
C46	MGT128_RX1_P	AC38	D46	MGT128_TX1_P	AA33
C47	MGT128_RX1_N	AC39	D47	MGT128_TX1_N	AA34
C48	GND	-	D48	GND	-
C49	MGT128_RX0_P	AD36	D49	MGT128_TX0_P	AB31
C50	MGT128_RX0_N	AD37	D50	MGT128_TX0_N	AB32
C51	GND	-	D51	GND	-
C52	SELECTMAP_DONE	AE24	D52	BOOT_M0	AE27
C53	SELECTMAP_INIT_B	AE26	D53	BOOT_M1	AF22
C54	GND	-	D54	GND	-
C55	NC	-	D55	BOOT_M2	AF24
C56	SELECTMAP_CCLK	AD23	D56	NC	-
C57	GND	-	D57	GND	-
C58	SELECTMAP_WR	AG22	D58	NC	-
C59	SELECTMAP_PROGRAM_B	AF26	D59	NC	-
C60	GND	-	D60	GND	-

Table 2.9.6 - J3 Connector Pin Assignment

J4 connector

J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
A1	VCCO_90_91_93_94	E2, F5, B8, F10, K12, N11, B13, G13	B1	POWER_SCL	-
A2	GND	-	B2	GND	-
A3	B94_L9_N	C12	B3	B94_L6_N	E11

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J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
A4	B94_L9_P	D12	B4	B94_L6_P	F11
A5	B94_L8_N	D13	B5	B94_L7_N	F12
A6	B94_L8_P	E13	B6	B94_L7_P	F13
A7	GND	-	B7	GND	-
A8	B71_L1_N	M15	B8	B71_L10_N	F14
A9	B71_L1_P	M16	B9	B71_L10_P	G15
A10	GND	-	B10	GND	-
A11	B71_L18_N	D15	B11	B71_L4_N	L16
A12	B71_L18_P	D16	B12	B71_L4_P	L17
A13	GND	-	B13	GND	-
A14	B71_L6_N	K14	B14	B71_L5_N	J16
A15	B71_L6_P	K15	B15	B71_L5_P	K16
A16	GND	-	B16	GND	-
A17	B71_L14_N	F16	B17	B71_L11_N	G16
A18	B71_L14_P	F17	B18	B71_L11_P	G17
A19	GND	-	B19	GND	-
A20	B70_L11_N	F21	B20	B70_L20_N	B20
A21	B70_L11_P	G21	B21	B70_L20_P	C20
A22	GND	-	B22	GND	-
A23	B70_L2_N	M20	B23	B70_L18_N	D20
A24	B70_L2_P	M19	B24	B70_L18_P	E20
A25	GND	-	B25	GND	-
A26	B70_L6_N	K21	B26	B70_L1_N	M22
A27	B70_L6_P	K20	B27	B70_L1_P	M21
A28	GND	-	B28	GND	-
A29	B70_L7_N	H22	B29	B70_L8_N	J21
A30	B70_L7_P	J22	B30	B70_L8_P	J20

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J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
A31	GND	-	B31	GND	-
A32	B70_L4_N	L22	B32	B70_L17_N	D21
A33	B70_L4_P	L21	B33	B70_L17_P	E21
A34	GND	-	B34	GND	-
A35	B70_L3_N	L24	B35	B70_L16_N	D23
A36	B70_L3_P	L23	B36	B70_L16_P	D22
A37	GND	-	B37	GND	-
A38	B70_L14_N	E24	B38	B70_L15_N	D25
A39	B70_L14_P	E23	B39	B70_L15_P	E25
A40	GND	-	B40	GND	-
A41	B70_L13_N	F24	B41	B70_L9_N	G24
A42	B70_L13_P	F23	B42	B70_L9_P	H24
A43	GND	-	B43	GND	-
A44	B69_L3_N	L27	B44	B69_L1_N	M26
A45	B69_L3_P	L26	B45	B69_L1_P	M25
A46	GND	-	B46	GND	-
A47	B69_L5_N	J26	B47	B69_L4_N	H25
A48	B69_L5_P	K26	B48	B69_L4_P	J25
A49	GND	-	B49	GND	-
A50	B69_L2_N	H27	B50	B69_L11_N	F27
A51	B69_L2_P	J27	B51	B69_L11_P	G27
A52	GND	-	B52	GND	-
A53	B69_L24_N	A29	B53	B69_L9_N	H28
A54	B69_L24_P	A28	B54	B69_L9_P	J28
A55	GND	-	B55	GND	-
A56	B69_L16_N	D30	B56	B69_L8_N	H30
A57	B69_L16_P	E30	B57	B69_L8_P	H29

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J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
A58	GND	-	B58	GND	-
A59	B69_L15_N	D31	B59	B69_L7_N	J31
A60	B69_L15_P	E31	B60	B69_L7_P	J30

Table 2.9.7 - J4 Connector Pin Assignment

J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
C1	POWER_SDA	-	D1	POWER_ALT	-
C2	GND	-	D2	GND	-
C3	B94_L4_N	G10	D3	B94_L2_N	J10
C4	B94_L4_P	H10	D4	B94_L2_P	J11
C5	B94_L1_N	J12	D5	B94_L3_N	H12
C6	B94_L1_P	J13	D6	B94_L3_P	H13
C7	GND	-	D7	GND	-
C8	B71_L16_N	E15	D8	B71_L24_N	A16
C9	B71_L16_P	E16	D9	B71_L24_P	B17
C10	GND	-	D10	GND	-
C11	B71_L20_N	C14	D11	B71_L23_N	A17
C12	B71_L20_P	C15	D12	B71_L23_P	A18
C13	GND	-	D13	GND	-
C14	B71_L22_N	B15	D14	B71_L9_N	G14
C15	B71_L22_P	B16	D15	B71_L9_P	H14
C16	GND	-	D16	GND	-
C17	B71_L7_N	H15	D17	B71_L8_N	H17
C18	B71_L7_P	J15	D18	B71_L8_P	H18
C19	GND	-	D19	GND	-
C20	B71_L13_N	F18	D20	B71_L12_N	G19
C21	B71_L13_P	F19	D21	B71_L12_P	H19

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J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
C22	GND	-	D22	GND	-
C23	B71_L3_N	K18	D23	B71_L19_N	C17
C24	B71_L3_P	L18	D24	B71_L19_P	C18
C25	GND	-	D25	GND	-
C26	B71_L21_N	A19	D26	B71_L17_N	D17
C27	B71_L21_P	B19	D27	B71_L17_P	D18
C28	GND	-	D28	GND	-
C29	B71_L2_N	K19	D29	B71_L15_N	E18
C30	B71_L2_P	L19	D30	B71_L15_P	E19
C31	GND	-	D31	GND	-
C32	B70_L10_N	G20	D32	B70_L21_N	A21
C33	B70_L10_P	H20	D33	B70_L21_P	B21
C34	GND	-	D34	GND	-
C35	B70_L12_N	F22	D35	B70_L22_N	A22
C36	B70_L12_P	G22	D36	B70_L22_P	B22
C37	GND	-	D37	GND	-
C38	B70_L24_N	A24	D38	B70_L5_N	K24
C39	B70_L24_P	A23	D39	B70_L5_P	K23
C40	GND	-	D40	GND	-
C41	B70_L19_N	C23	D41	B70_L23_N	B25
C42	B70_L19_P	C22	D42	B70_L23_P	B24
C43	GND	-	D43	GND	-
C44	B69_L6_N	G26	D44	B69_L13_N	F29
C45	B69_L6_P	G25	D45	B69_L13_P	F28
C46	GND	-	D46	GND	-
C47	B69_L17_N	D26	D47	B69_L14_N	E29
C48	B69_L17_P	E26	D48	B69_L14_P	E28

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J4 pin	Signal name	Pin number	J4 pin	Signal name	Pin number
C49	GND	-	D49	GND	-
C50	B69_L18_N	D28	D50	B69_L22_N	A27
C51	B69_L18_P	D27	D51	B69_L22_P	B27
C52	GND	-	D52	GND	-
C53	B69_L20_N	C28	D53	B69_L19_N	B29
C54	B69_L20_P	C27	D54	B69_L19_P	C29
C55	GND	-	D55	GND	-
C56	B69_L12_N	G30	D56	B69_L23_N	A26
C57	B69_L12_P	G29	D57	B69_L23_P	B26
C58	GND	-	D58	GND	-
C59	B69_L10_N	F31	D59	B69_L21_N	A31
C60	B69_L10_P	G31	D60	B69_L21_P	B31

Table 2.9.8 - J4 Connector Pin Assignment

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Chapter 3 Carrier Board

3.1 Introduction

This chapter provides a detailed introduction to carrier boards.

- PCIe 3.0 x16 interface
- 1 gigabit network interface
- 2- channel FMC HPC interface
- 2-channel MIPI input interface
- USB UART interface
- Micro SD Card Slot
- 1 SATA interfaces
- 40-pin expansion port
- JTAG debug port
- LED
- Button

3.2 PCIe

The AXKU15S carrier board has a PCIe x16 interface that supports the PCIe Gen3.0 protocol. 16 pairs of transceivers connect to the gold fingers of the PCIe x16 for data communication.

The PCIe interface transmits and receives signals directly to the FPGA BANK228~231 transceiver. The 16 TX and RX signals are connected to the FPGA transceiver in a differential signal manner, and the single-channel communication rate can reach up to 8 Gbps .

The design schematic of the PCIe interface of the development board is shown in the figure below , where the TX signal is connected using AC coupling mode.

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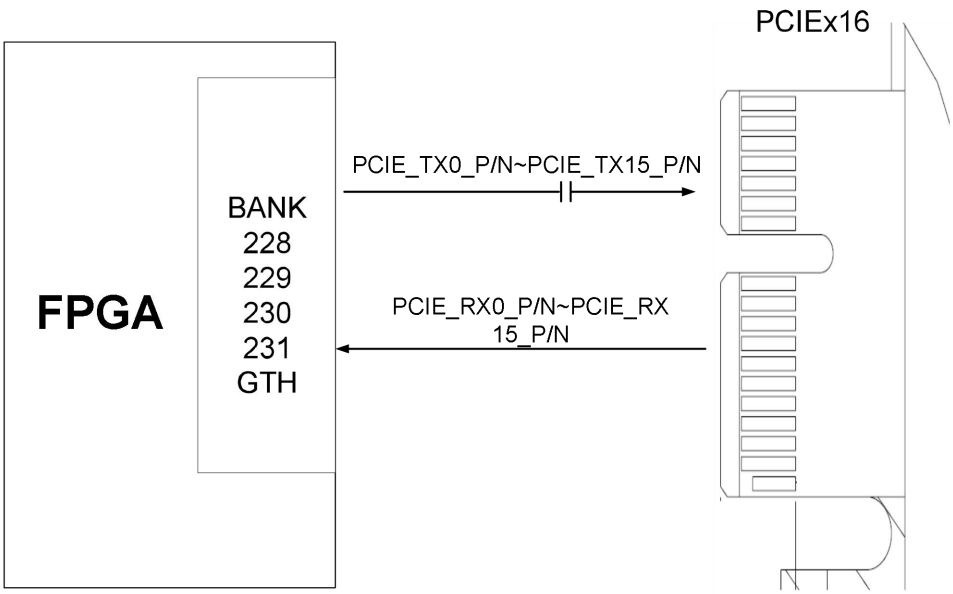


Figure 3.2.1 - Schematic diagram of PCIe slot design

The pin assignments for the PCIe x16 interface FPGA are as follows:

Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
PCIE_RX0_P	MGTHRXP3_231	H2	PCIE Channel 0 Data Receive Positive
PCIE_RX0_N	MGTHRXN3_231	H1	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	MGTHRXP2_231	J4	PCIE Channel 1 Data Receive Positive
PCIE_RX1_N	MGTHRXN2_231	J3	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	MGTHRXP1_231	K2	PCIE Channel 2 Data Receive Positive
PCIE_RX2_N	MGTHRXN1_231	K1	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	MGTHRXP0_231	L4	PCIE Channel 3 Data Receive Positive
PCIE_RX3_N	MGTHRXN0_231	L3	PCIE Channel 3 Data Receive Negative
PCIE_RX4_P	MGTHRXP3_230	M2	PCIE Channel 4 Data Receive Positive
PCIE_RX4_N	MGTHRXN3_230	M1	PCIE Channel 4 Data Receive Negative
PCIE_RX5_P	MGTHRXP2_230	N4	PCIE Channel 5 Data Receive Positive
PCIE_RX5_N	MGTHRXN2_230	N3	PCIE Channel 5 Data Receive Negative
PCIE_RX6_P	MGTHRXP1_230	P2	PCIE Channel 6 Data Receive Positive
PCIE_RX6_N	MGTHRXN1_230	P1	PCIE Channel 6 Data Receive Negative
PCIE_RX7_P	MGTHRXP0_230	R4	PCIE Channel 7 Data Receive Positive

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
PCIE_RX7_N	MGTHRXN0_230	R3	PCIE Channel 7 Data Receive Negative
PCIE_RX8_P	MGTHRXP3_229	T2	PCIE Channel 8 Data Receive Positive
PCIE_RX8_N	MGTHRXN3_229	T1	PCIE Channel 8 Data Receive Negative
PCIE_RX9_P	MGTHRXP2_229	U4	PCIE Channel 9 Data Receive Positive
PCIE_RX9_N	MGTHRXN2_229	U3	PCIE Channel 9 Data Receive Negative
PCIE_RX10_P	MGTHRXP1_229	V2	PCIE Channel 10 Data Receive Positive
PCIE_RX10_N	MGTHRXN1_229	V1	PCIE Channel 10 Data Receive Negative
PCIE_RX11_P	MGTHRXP0_229	W4	PCIE Channel 11 Data Receive Positive
PCIE_RX11_N	MGTHRXN0_229	W3	PCIE Channel 11 Data Receive Negative
PCIE_RX12_P	MGTHRXP3_228	Y2	PCIE Channel 12 Data Receive Positive
PCIE_RX12_N	MGTHRXN3_228	Y1	PCIE Channel 12 Data Receive Negative
PCIE_RX13_P	MGTHRXP2_228	AA4	PCIE Channel 13 Data Receive Positive
PCIE_RX13_N	MGTHRXN2_228	AA3	PCIE Channel 13 Data Receive Negative
PCIE_RX14_P	MGTHRXP1_228	AB2	PCIE Channel 14 Data Receive Positive
PCIE_RX14_N	MGTHRXN1_228	AB1	PCIE Channel 14 Data Receive Negative
PCIE_RX15_P	MGTHRXP0_228	AC4	PCIE Channel 15 Data Receive Positive
PCIE_RX15_N	MGTHRXN0_228	AC3	PCIE Channel 15 Data Receive Negative
PCIE_TX0_P	MGTHTXP3_231	H6	PCIE Channel 0 Data Transmit Positive
PCIE_TX0_N	MGTHTXN3_231	H5	PCIE Channel 0 Data Transmit Negative
PCIE_TX1_P	MGTHTXP2_231	J8	PCIE Channel 1 Data Transmit Positive
PCIE_TX1_N	MGTHTXN2_231	J7	PCIE Channel 1 Data Transmit Negative
PCIE_TX2_P	MGTHTXP1_231	K6	PCIE Channel 2 Data Transmit Positive
PCIE_TX2_N	MGTHTXN1_231	K5	PCIE Channel 2 Data Transmit Negative
PCIE_TX3_P	MGTHTXP0_231	L8	PCIE Channel 3 Data Transmit Positive
PCIE_TX3_N	MGTHTXN0_231	L7	PCIE Channel 3 Data Transmit Negative
PCIE_TX4_P	MGTHTXP3_230	M6	PCIE Channel 4 Data Transmit Positive
PCIE_TX4_N	MGTHTXN3_230	M5	PCIE Channel 4 Data Transmit Negative

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
PCIE_TX5_P	MGTHTXP2_230	N8	PCIE Channel 5 Data Transmit Positive
PCIE_TX5_N	MGTHTXN2_230	N7	PCIE Channel 5 Data Transmit Negative
PCIE_TX6_P	MGTHTXP1_230	P6	PCIE Channel 6 Data Transmit Positive
PCIE_TX6_N	MGTHTXN1_230	P5	PCIE Channel 6 Data Transmit Negative
PCIE_TX7_P	MGTHTXP0_230	R8	PCIE Channel 7 Data Transmit Positive
PCIE_TX7_N	MGTHTXN0_230	R7	PCIE Channel 7 Data Transmit Negative
PCIE_TX8_P	MGTHTXP3_229	T6	PCIE Channel 8 Data Transmit Positive
PCIE_TX8_N	MGTHTXN3_229	T5	PCIE Channel 8 Data Transmit Negative
PCIE_TX9_P	MGTHTXP2_229	U8	PCIE Channel 9 Data Transmit Positive
PCIE_TX9_N	MGTHTXN2_229	U7	PCIE Channel 9 Data Transmit Negative
PCIE_TX10_P	MGTHTXP1_229	V6	PCIE Channel 10 Data Transmit Positive
PCIE_TX10_N	MGTHTXN1_229	V5	PCIE Channel 10 Data Transmit Negative
PCIE_TX11_P	MGTHTXP0_229	W8	PCIE Channel 11 Data Transmit Positive
PCIE_TX11_N	MGTHTXN0_229	W7	PCIE Channel 11 Data Transmit Negative
PCIE_TX12_P	MGTHTXP3_228	Y6	PCIE Channel 12 Data Transmit Positive
PCIE_TX12_N	MGTHTXN3_228	Y5	PCIE Channel 12 Data Transmit Negative
PCIE_TX13_P	MGTHTXP2_228	AA8	PCIE Channel 13 Data Transmit Positive
PCIE_TX13_N	MGTHTXN2_228	AA7	PCIE Channel 13 Data Transmit Negative
PCIE_TX14_P	MGTHTXP1_228	AB6	PCIE Channel 14 Data Transmit Positive
PCIE_TX14_N	MGTHTXN1_228	AB5	PCIE Channel 14 Data Transmit Negative
PCIE_TX15_P	MGTHTXP0_228	AC8	PCIE Channel 15 Data Transmit Positive
PCIE_TX15_N	MGTHTXN0_228	AC7	PCIE Channel 15 Data Transmit Negative
PCIE_CLK_P	MGTREFCLK0P_229	AA12	PCIE Channel Reference Clock Positive
PCIE_CLK_N	MGTREFCLK0N_229	AA11	PCIE Channel Reference Clock Negative
FPGA_PCIE_PERST_n	IO_T3U_N12_PERSTN0_65	AP10	PCIE Reset Signal

Table 3.2.1 - PCIe x16 Pin Assignment

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3.3 Gigabit Ethernet Interface

The development board uses a JL2121D chip. The Ethernet PHY chip provides network communication services to users. It connects to the FPGA 's I/O interface. The JL2121D chip supports 10/100/1000 Mbps network transmission rates and communicates with the FPGA via the RGMII interface . The JL2121D chip supports MDI/MDX auto-adaptation, various speed auto-adaptation, Master/Slave auto-adaptation, and MDIO bus for PHY register management.

JL2121D detects the voltage levels of specific I/O pins to determine its operating mode . The table below describes the default settings of the GPHY chip after power-up.

Configure Pin	illustrate	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address in MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock 2ns delay	Delay
RXD0_RXDLY	RX clock 2ns delay	Delay

Table 3.3.1-G PHY chip default configuration

When the network is connected to Gigabit Ethernet, the FPGA and PHY chip JL2121 communicate via the RGMII bus for data transmission. The transmission clock is 125 MHz , and the data is sampled on the rising and falling edges of the clock .

When the network is connected to a 100 Mbps Ethernet network, data transmission between the FPGA and the JL2121 PHY chip is conducted via the RMII bus, with a transmission clock of 25 MHz . Data is sampled on both the rising and falling edges of the clock . Figure 3.3.1 shows a schematic diagram of the connection between the FPGA and the Ethernet PHY chip.

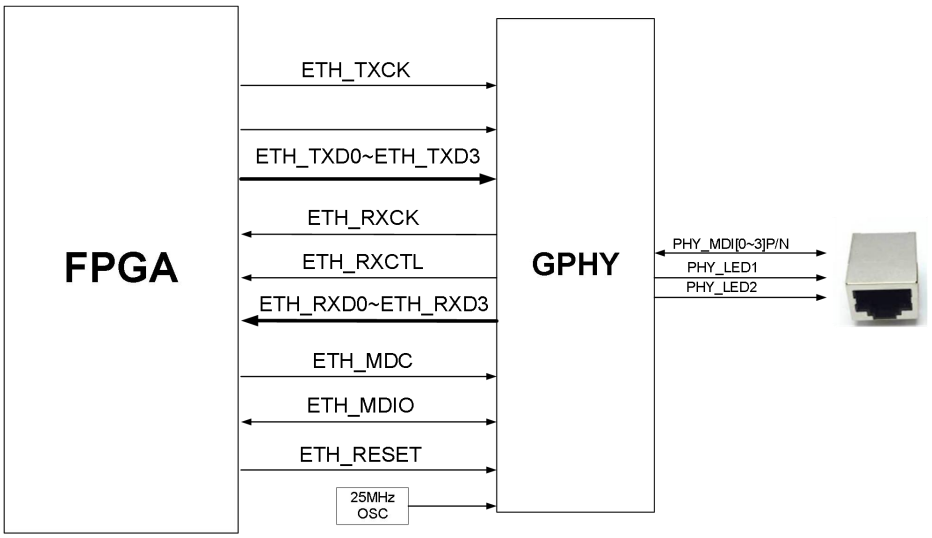


Figure 3.3.1 - Schematic diagram of Gigabit Ethernet interface connection

The FPGA pin assignments for the Ethernet PHY are as follows:

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Signal name	FPGA pin names	FPGA pin numbers	Remark
ETH_MDC	IO_L1N_T0L_N1_DBC_RS1_65	AW10	MDIO manages the clock
ETH_MDIO	IO_L1P_T0L_N0_DBC_RS0_65	AW11	MDIO Management Data
ETH_RESET	IO_L24P_T3U_N10_64	AM18	PHY chip reset
ETH_RXCK	IO_L11P_T1U_N8_GC_A10_D26_65	AR14	RGMII Receive Clock
ETH_RXCTL	IO_L11N_T1U_N9_GC_A11_D27_65	AT14	Received data valid signal
ETH_RXD0	IO_L18N_T2U_N11_AD2N_D13_65	AL16	Received data Bit 0
ETH_RXD1	IO_L18P_T2U_N10_AD2P_D12_65	AK16	Receive data Bit1
ETH_RXD2	IO_L20N_T3L_N3_AD1N_D09_65	AP13	Receive data Bit 2
ETH_RXD3	IO_L20P_T3L_N2_AD1P_D08_65	AN13	Receive data Bit 3
ETH_TXCK	IO_L23P_T3U_N8_I2C_SCLK_65	AP11	RGMII Transmit Clock
ETH_TXCTL	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65	AR11	Send enable signal
ETH_TXD0	IO_L15P_T2L_N4_AD11P_A02_D18_65	AJ14	Send data bit 0
ETH_TXD1	IO_L15N_T2L_N5_AD11N_A03_D19_65	AK14	Send data bit 1
ETH_TXD2	IO_L6P_T0U_N10_AD6P_A20_65	AU14	Send data bit 2
ETH_TXD3	IO_L6N_T0U_N11_AD6N_A21_65	AU13	Send data bit 3

Table 3.3.2 - Ethernet PHY Pin Assignments

3.4 FMC HPC Interface

The development board has two FMC HPC expansion ports , namely FMC1 (J12) and FMC2 (J13) , which can be connected to various FMC modules from Xilinx or our Alinx (HDMI input/output modules, binocular camera modules, high-speed AD modules, etc.).

The FMC 1 expansion port includes 34 pairs of LA signal differential pairs, 2 pairs of clock signals, and 24 pairs of HA signals , which are connected to FPGA chips BANK6 9 , BANK70 , and BANK71 respectively . The default voltage level is 1.8V. Eight high-speed GTH transceiver signals are connected to the I/O pins of FPGA chips BANK226 and BANK227. The schematic diagram of the FPGA and FMC HPC connector is shown in the figure .

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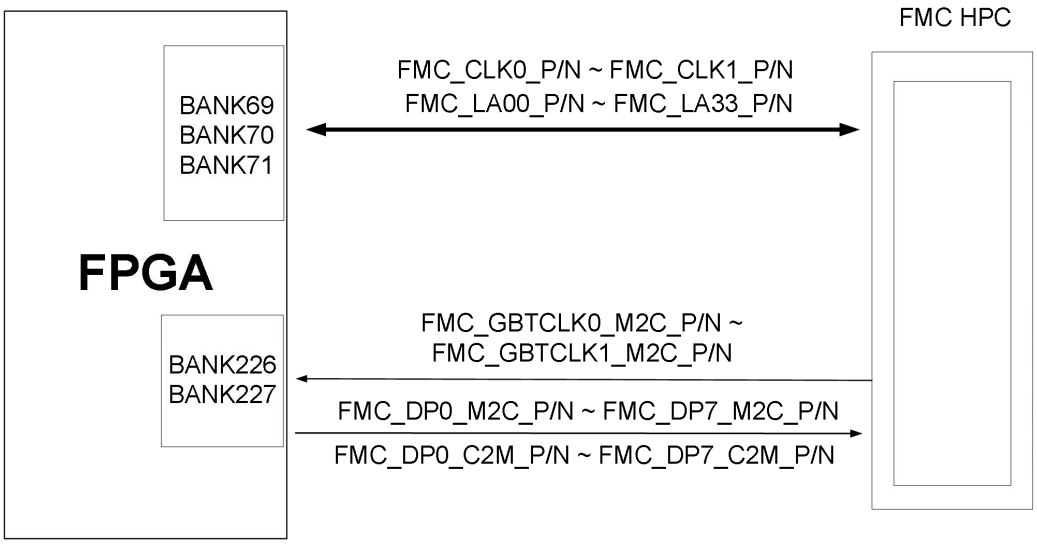


Figure 3.4.1 - Schematic diagram of FMC HPC connector

The pin assignments for the FMC HPC J12 connector are as follows:

Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_CLK0_N	B70_L11_N	F21	FMC Channel 0 Input Reference Clock N
FMC1_CLK0_P	B70_L11_P	G21	FMC Channel 0 Input Reference Clock P
FMC1_CLK1_N	B69_L12_N	G30	FMC Channel 1 Input Reference Clock N
FMC1_CLK1_P	B69_L12_P	G29	FMC Channel 1 Input Reference Clock P
FMC1_LA00_CC_N	B70_L14_N	E24	FMC LA Channel 0 Data (Clock) N
FMC1_LA00_CC_P	B70_L14_P	E23	FMC LA Channel 0 Data (Clock) P
FMC1_LA01_CC_N	B70_L13_N	F24	FMC LA Channel 1 Data (Clock) N
FMC1_LA01_CC_P	B70_L13_P	F23	FMC LA Channel 1 Data (Clock) P
FMC1_LA02_N	B70_L17_N	D21	FMC LA Channel 2 Data N
FMC1_LA02_P	B70_L17_P	E21	FMC LA Channel 2 Data P
FMC1_LA03_N	B70_L24_N	A24	FMC LA Channel 3 Data N
FMC1_LA03_P	B70_L24_P	A23	FMC LA Channel 3 Data P
FMC1_LA04_N	B70_L12_N	F22	FMC LA Channel 4 Data N
FMC1_LA04_P	B70_L12_P	G22	FMC LA Channel 4 Data P
FMC1_LA05_N	B70_L6_N	K21	FMC LA Channel 5 Data N
FMC1_LA05_P	B70_L6_P	K20	FMC LA Channel 5 Data P

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_LA06_N	B70_L5_N	K24	FMC LA Channel 6 Data P
FMC1_LA06_P	B70_L5_P	K23	FMC LA Channel 6 Data P
FMC1_LA07_N	B70_L4_N	L22	FMC LA Channel 7 Data N
FMC1_LA07_P	B70_L4_P	L21	FMC LA Channel 7 Data P
FMC1_LA08_N	B70_L3_N	L24	FMC LA Channel 8 Data N
FMC1_LA08_P	B70_L3_P	L23	FMC LA Channel 8 Data P
FMC1_LA09_N	B70_L2_N	M20	FMC LA Channel 9 Data N
FMC1_LA09_P	B70_L2_P	M19	FMC LA Channel 9 Data P
FMC1_LA10_N	B70_L18_N	D20	FMC LA Channel 10 Data N
FMC1_LA10_P	B70_L18_P	E20	FMC LA Channel 10 Data P
FMC1_LA11_N	B70_L23_N	B25	FMC LA Channel 11 Data N
FMC1_LA11_P	B70_L23_P	B24	FMC LA Channel 11 Data P
FMC1_LA12_N	B70_L1_N	M22	FMC LA Channel 12 Data N
FMC1_LA12_P	B70_L1_P	M21	FMC LA Channel 12 Data P
FMC1_LA13_N	B70_L21_N	A21	FMC LA Channel 13 Data N
FMC1_LA13_P	B70_L21_P	B21	FMC LA Channel 13 Data P
FMC1_LA14_N	B70_L19_N	C23	FMC LA Channel 14 Data N
FMC1_LA14_P	B70_L19_P	C22	FMC LA Channel 14 Data P
FMC1_LA15_N	B70_L20_N	B20	FMC LA Channel 15 Data N
FMC1_LA15_P	B70_L20_P	C20	FMC LA Channel 15 Data P
FMC1_LA16_N	B70_L22_N	A22	FMC LA Channel 16 Data N
FMC1_LA16_P	B70_L22_P	B22	FMC LA Channel 16 Data P
FMC1_LA17_CC_N	B69_L14_N	E29	FMC LA Channel 17 Data (Clock) N
FMC1_LA17_CC_P	B69_L14_P	E28	FMC LA Channel 17 Data (Clock) P
FMC1_LA18_CC_N	B69_L13_N	F29	FMC LA Channel 18 Data (Clock) N
FMC1_LA18_CC_P	B69_L13_P	F28	FMC LA Channel 18 Data (Clock) P
FMC1_LA19_N	B70_L7_N	H22	FMC LA Channel 19 Data N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_LA19_P	B70_L7_P	J22	FMC LA Channel 19 Data P
FMC1_LA20_N	B69_L17_N	D26	FMC LA Channel 20 Data N
FMC1_LA20_P	B69_L17_P	E26	FMC LA Channel 20 Data P
FMC1_LA21_N	B69_L2_N	H27	FMC LA Channel 21 Data N
FMC1_LA21_P	B69_L2_P	J27	FMC LA Channel 21 Data P
FMC1_LA22_N	B69_L4_N	H25	FMC LA Channel 22 Data N
FMC1_LA22_P	B69_L4_P	J25	FMC LA Channel 22 Data P
FMC1_LA23_N	B69_L5_N	J26	FMC LA Channel 23 Data N
FMC1_LA23_P	B69_L5_P	K26	FMC LA Channel 23 Data P
FMC1_LA24_N	B69_L15_N	D31	FMC LA Channel 24 Data N
FMC1_LA24_P	B69_L15_P	E31	FMC LA Channel 24 Data P
FMC1_LA25_N	B70_L8_N	J21	FMC LA Channel 25 Data N
FMC1_LA25_P	B70_L8_P	J20	FMC LA Channel 25 Data P
FMC1_LA26_N	B69_L1_N	M26	FMC LA Channel 26 Data N
FMC1_LA26_P	B69_L1_P	M25	FMC LA Channel 26 Data P
FMC1_LA27_N	B69_L3_N	L27	FMC LA Channel 27 Data N
FMC1_LA27_P	B69_L3_P	L26	FMC LA Channel 27 Data P
FMC1_LA28_N	B69_L16_N	D30	FMC LA Channel 28 Data N
FMC1_LA28_P	B69_L16_P	E30	FMC LA Channel 28 Data P
FMC1_LA29_N	B69_L7_N	J31	FMC LA Channel 29 Data N
FMC1_LA29_P	B69_L7_P	J30	FMC LA Channel 29 Data P
FMC1_LA30_N	B69_L11_N	F27	FMC LA Channel 30 Data N
FMC1_LA30_P	B69_L11_P	G27	FMC LA Channel 30 Data P
FMC1_LA31_N	B69_L9_N	H28	FMC LA Channel 31 Data N
FMC1_LA31_P	B69_L9_P	J28	FMC LA Channel 31 Data P
FMC1_LA32_N	B69_L10_N	F31	FMC LA Channel 32 Data N
FMC1_LA32_P	B69_L10_P	G31	FMC LA Channel 32 Data P

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_LA33_N	B69_L8_N	H30	FMC LA Channel 33 Data N
FMC1_LA33_P	B69_L8_P	H29	FMC LA Channel 33 Data P
FMC1_SCL	B90_L1_P	E5	FMC I2C Bus Clock
FMC1_SDA	B90_L1_N	E4	FMC I2C Bus Data
FMC1_HA00_CC_N	B71_L13_N	F18	FMC HA Channel 0 Data (Clock) N
FMC1_HA00_CC_P	B71_L13_P	F19	FMC HA Channel 0 Data (Clock) P
FMC1_HA01_CC_N	B71_L11_N	G16	FMC HA Channel 1 Data (Clock) N
FMC1_HA01_CC_P	B71_L11_P	G17	FMC HA Channel 1 Data (Clock) P
FMC1_HA02_N	B71_L21_N	A19	FMC HA Channel 2 Data N
FMC1_HA02_P	B71_L21_P	B19	FMC HA Channel 2 Data P
FMC1_HA03_N	B71_L12_N	G19	FMC HA Channel 3 Data N
FMC1_HA03_P	B71_L12_P	H19	FMC HA Channel 3 Data P
FMC1_HA04_N	B71_L22_N	B15	FMC HA Channel 4 Data N
FMC1_HA04_P	B71_L22_P	B16	FMC HA Channel 4 Data P
FMC1_HA05_N	B71_L19_N	C17	FMC HA Channel 5 Data N
FMC1_HA05_P	B71_L19_P	C18	FMC HA Channel 5 Data P
FMC1_HA06_N	B71_L9_N	G14	FMC HA Channel 6 Data N
FMC1_HA06_P	B71_L9_P	H14	FMC HA Channel 6 Data P
FMC1_HA07_N	B71_L6_N	K14	FMC HA Channel 7 Data N
FMC1_HA07_P	B71_L6_P	K15	FMC HA Channel 7 Data P
FMC1_HA08_N	B71_L15_N	E18	FMC HA Channel 8 Data N
FMC1_HA08_P	B71_L15_P	E19	FMC HA Channel 8 Data P
FMC1_HA09_N	B71_L17_N	D17	FMC HA Channel 9 Data N
FMC1_HA09_P	B71_L17_P	D18	FMC HA Channel 9 Data P
FMC1_HA10_N	B71_L8_N	H17	FMC HA Channel 10 Data N
FMC1_HA10_P	B71_L8_P	H18	FMC HA Channel 10 Data P
FMC1_HA11_N	B71_L16_N	E15	FMC HA Channel 11 Data N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_HA11_P	B71_L16_P	E16	FMC HA Channel 11 Data P
FMC1_HA12_N	B71_L18_N	D15	FMC HA Channel 12 Data N
FMC1_HA12_P	B71_L18_P	D16	FMC HA Channel 12 Data P
FMC1_HA13_N	B71_L10_N	F14	FMC HA Channel 13 Data N
FMC1_HA13_P	B71_L10_P	G15	FMC HA Channel 13 Data P
FMC1_HA14_N	B71_L23_N	A17	FMC HA Channel 14 Data N
FMC1_HA14_P	B71_L23_P	A18	FMC HA Channel 14 Data P
FMC1_HA15_N	B71_L24_N	A16	FMC HA Channel 15 Data N
FMC1_HA15_P	B71_L24_P	B17	FMC HA Channel 15 Data P
FMC1_HA16_N	B71_L20_N	C14	FMC HA Channel 16 Data N
FMC1_HA16_P	B71_L20_P	C15	FMC HA Channel 16 Data P
FMC1_HA17_CC_N	B71_L14_N	F16	FMC HA Channel 17 Data (Clock) N
FMC1_HA17_CC_P	B71_L14_P	F17	FMC HA Channel 17 Data (Clock) P
FMC1_HA18_N	B70_L9_N	G24	FMC HA Channel 18 Data N
FMC1_HA18_P	B70_L9_P	H24	FMC HA Channel 18 Data P
FMC1_HA19_N	B70_L10_N	G20	FMC HA Channel 19 Data N
FMC1_HA19_P	B70_L10_P	H20	FMC HA Channel 19 Data P
FMC1_HA20_N	B71_L7_N	H15	FMC HA Channel 20 Data N
FMC1_HA20_P	B71_L7_P	J15	FMC HA Channel 20 Data P
FMC1_HA21_N	B70_L15_N	D25	FMC HA Channel 21 Data N
FMC1_HA21_P	B70_L15_P	E25	FMC HA Channel 21 Data P
FMC1_HA22_N	B70_L16_N	D23	FMC HA Channel 22 Data N
FMC1_HA22_P	B70_L16_P	D22	FMC HA Channel 22 Data P
FMC1_HA23_N	B69_L24_N	A29	FMC HA Channel 23 Data N
FMC1_HA23_P	B69_L24_P	A28	FMC HA Channel 23 Data P
FMC1_HPC_GBTCLK0_M2C_C_P	MGT226_CLK0_P	AG12	Transceiver Reference Clock 0 Input P
FMC1_HPC_GBTCLK0_M2C_C_N	MGT226_CLK0_N	AG11	Transceiver Reference Clock 0 Input N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_DP0_M2C_P	MGT226_RX0_P	AL4	Transceiver Data 0 Input P
FMC1_DP0_M2C_N	MGT226_RX0_N	AL3	Transceiver Data 0 Input N
FMC1_DP1_M2C_P	MGT226_RX1_P	AK2	Transceiver Data 1 Input P
FMC1_DP1_M2C_N	MGT226_RX1_N	AK1	Transceiver Data 1 Input N
FMC1_DP2_M2C_P	MGT226_RX2_P	AJ4	Transceiver Data 2 Input P
FMC1_DP2_M2C_N	MGT226_RX2_N	AJ3	Transceiver Data 2 Input N
FMC1_DP3_M2C_P	MGT226_RX3_P	AH2	Transceiver Data 3 Input P
FMC1_DP3_M2C_N	MGT226_RX3_N	AH1	Transceiver Data 3 Input N
FMC1_DP4_M2C_P	MGT227_RX0_P	AG4	Transceiver Data 4 Input P
FMC1_DP4_M2C_N	MGT227_RX0_N	AG3	Transceiver Data 4 Input N
FMC1_DP5_M2C_P	MGT227_RX1_P	AF2	Transceiver Data 5 Input P
FMC1_DP5_M2C_N	MGT227_RX1_N	AF1	Transceiver Data 5 Input N
FMC1_DP6_M2C_P	MGT227_RX2_P	AE4	Transceiver Data 6 Input P
FMC1_DP6_M2C_N	MGT227_RX2_N	AE3	Transceiver Data 6 Input N
FMC1_DP7_M2C_P	MGT227_RX3_P	AD2	Transceiver Data 7 Input P
FMC1_DP7_M2C_N	MGT227_RX3_N	AD1	Transceiver Data 7 Input N
FMC1_DP0_C2M_P	MGT226_TX0_P	AL8	Transceiver Data 0 Output P
FMC1_DP0_C2M_N	MGT226_TX0_N	AL7	Transceiver Data 0 Output N
FMC1_DP1_C2M_P	MGT226_TX1_P	AK6	Transceiver Data 1 Output P
FMC1_DP1_C2M_N	MGT226_TX1_N	AK5	Transceiver Data 1 Output N
FMC1_DP2_C2M_P	MGT226_TX2_P	AJ8	Transceiver Data 2 Output P
FMC1_DP2_C2M_N	MGT226_TX2_N	AJ7	Transceiver Data 2 Output N
FMC1_DP3_C2M_P	MGT226_TX3_P	AH6	Transceiver Data 3 Output P
FMC1_DP3_C2M_N	MGT226_TX3_N	AH5	Transceiver Data 3 Output N
FMC1_DP4_C2M_P	MGT227_TX0_P	AG8	Transceiver Data 4 Output P
FMC1_DP4_C2M_N	MGT227_TX0_N	AG7	Transceiver Data 4 Output N
FMC1_DP5_C2M_P	MGT227_TX1_P	AF6	Transceiver Data 5 Output P

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC1_DP5_C2M_N	MGT227_TX1_N	AF5	Transceiver Data 5 Output N
FMC1_DP6_C2M_P	MGT227_TX2_P	AE8	Transceiver Data 6 Output P
FMC1_DP6_C2M_N	MGT227_TX2_N	AE7	Transceiver Data 6 Output N
FMC1_DP7_C2M_P	MGT227_TX3_P	AD6	Transceiver Data 7 Output P
FMC1_DP7_C2M_N	MGT227_TX3_N	AD5	Transceiver Data 7 Output N
FMC1_HPC_GBTCLK1_M2C_C_P	MGT227_CLK0_P	AE12	Transceiver Reference Clock 0 Input P
FMC1_HPC_GBTCLK1_M2C_C_N	MGT227_CLK0_N	AE11	Transceiver Reference Clock 0 Input N

Table 3.4.1 - FMC HPC J12 Connector Pin Assignment

The FMC2 expansion port contains 34 pairs of LA signal differential pairs and 2 pairs of clock signals , which are connected to FPGA chips BANK64 and BANK65 respectively. The default voltage level is 1.8V. Eight high-speed GTH transceiver signals are connected to the I/O pins of FPGA chips BANK224 and BANK225 .

The schematic diagrams of the FPGA and FMC HPC connectors are shown in Figure 3.4.2:

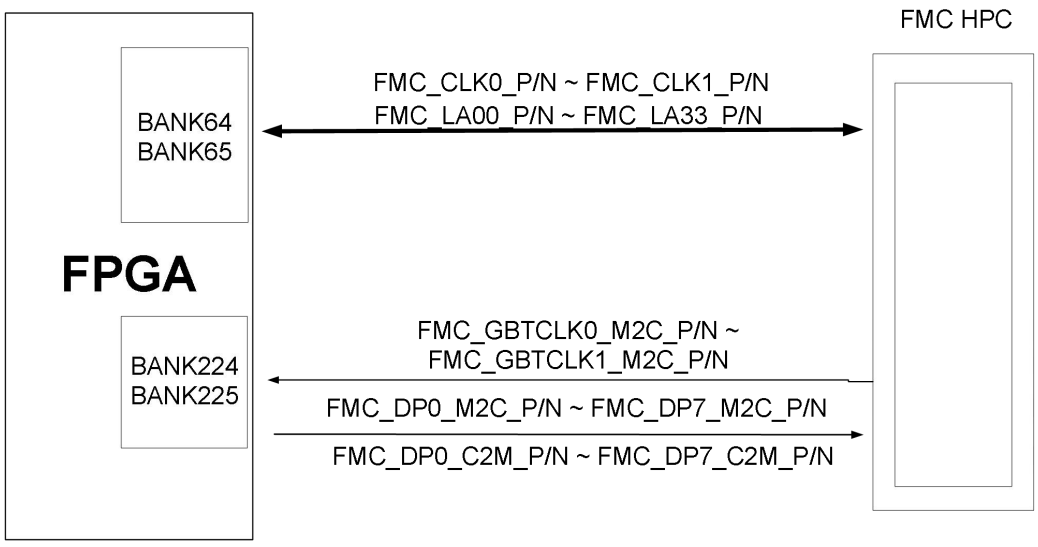


Figure 3.4.2 - Schematic diagram of HPC FMC connection

The pin assignments for the FMC HPC J13 connector are as follows:

Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC2_CLK0_M2C_N	B65_L12_N	AP14	FMC Channel 0 Input Reference Clock N
FMC2_CLK0_M2C_P	B65_L12_P	AP15	FMC Channel 0 Input Reference Clock P
FMC2_CLK1_M2C_N	B64_L12_N	AM20	FMC Channel 1 Input Reference Clock N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC2_CLK1_M2C_P	B64_L12_P	AL20	FMC Channel 1 Input Reference Clock P
FMC2_LA00_CC_N	B65_L14_N	AN15	FMC LA Channel 0 Data (Clock) N
FMC2_LA00_CC_P	B65_L14_P	AM15	FMC LA Channel 0 Data (Clock) P
FMC2_LA01_CC_N	B65_L13_N	AL14	FMC LA Channel 1 Data (Clock) N
FMC2_LA01_CC_P	B65_L13_P	AL15	FMC LA Channel 1 Data (Clock) P
FMC2_LA02_N	B65_L17_N	AJ15	FMC LA Channel 2 Data N
FMC2_LA02_P	B65_L17_P	AJ16	FMC LA Channel 2 Data P
FMC2_LA03_N	B65_L5_N	AV12	FMC LA Channel 3 Data N
FMC2_LA03_P	B65_L5_P	AV13	FMC LA Channel 3 Data P
FMC2_LA04_N	B65_L19_N	AT11	FMC LA Channel 4 Data N
FMC2_LA04_P	B65_L19_P	AT12	FMC LA Channel 4 Data P
FMC2_LA05_N	B65_L24_N	AM13	FMC LA Channel 5 Data N
FMC2_LA05_P	B65_L24_P	AM14	FMC LA Channel 5 Data P
FMC2_LA06_N	B65_L8_N	AU15	FMC LA Channel 6 Data N
FMC2_LA06_P	B65_L8_P	AT15	FMC LA Channel 6 Data P
FMC2_LA07_N	B65_L10_N	AR16	FMC LA Channel 7 Data N
FMC2_LA07_P	B65_L10_P	AP16	FMC LA Channel 7 Data P
FMC2_LA08_N	B65_L11_N	AL17	FMC LA Channel 8 Data N
FMC2_LA08_P	B65_L11_P	AK17	FMC LA Channel 8 Data P
FMC2_LA09_N	B65_L9_N	AW15	FMC LA Channel 9 Data N
FMC2_LA09_P	B65_L9_P	AV15	FMC LA Channel 9 Data P
FMC2_LA10_N	B65_L4_N	AV10	FMC LA Channel 10 Data N
FMC2_LA10_P	B65_L4_P	AU10	FMC LA Channel 10 Data P
FMC2_LA11_N	B64_L10_N	AL21	FMC LA Channel 11 Data N
FMC2_LA11_P	B64_L10_P	AK21	FMC LA Channel 11 Data P
FMC2_LA12_N	B65_L7_N	AW16	FMC LA Channel 12 Data N
FMC2_LA12_P	B65_L7_P	AV16	FMC LA Channel 12 Data P
FMC2_LA13_N	B64_L9_N	AP20	FMC LA Channel 13 Data N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC2_LA13_P	B64_L9_P	AP21	FMC LA Channel 13 Data P
FMC2_LA14_N	B64_L7_N	AR21	FMC LA Channel 14 Data N
FMC2_LA14_P	B64_L7_P	AR22	FMC LA Channel 14 Data P
FMC2_LA15_N	B64_L11_N	AN20	FMC LA Channel 15 Data N
FMC2_LA15_P	B64_L11_P	AN21	FMC LA Channel 15 Data P
FMC2_LA16_N	B64_L8_N	AM22	FMC LA Channel 16 Data N
FMC2_LA16_P	B64_L8_P	AL22	FMC LA Channel 16 Data P
FMC2_LA17_CC_N	B64_L14_N	AP18	FMC LA Channel 17 Data (Clock) N
FMC2_LA17_CC_P	B64_L14_P	AN18	FMC LA Channel 17 Data (Clock) P
FMC2_LA18_CC_N	B64_L13_N	AR19	FMC LA Channel 18 Data (Clock) N
FMC2_LA18_CC_P	B64_L13_P	AP19	FMC LA Channel 18 Data (Clock) P
FMC2_LA19_N	B64_L6_N	AW18	FMC LA Channel 19 Data N
FMC2_LA19_P	B64_L6_P	AV18	FMC LA Channel 19 Data P
FMC2_LA20_N	B64_L16_N	AU17	FMC LA Channel 20 Data N
FMC2_LA20_P	B64_L16_P	AT17	FMC LA Channel 20 Data P
FMC2_LA21_N	B64_L20_N	AM19	FMC LA Channel 21 Data N
FMC2_LA21_P	B64_L20_P	AL19	FMC LA Channel 21 Data P
FMC2_LA22_N	B64_L21_N	AJ19	FMC LA Channel 22 Data N
FMC2_LA22_P	B64_L21_P	AJ20	FMC LA Channel 22 Data P
FMC2_LA23_N	B64_L23_N	AJ18	FMC LA Channel 23 Data N
FMC2_LA23_P	B64_L23_P	AH18	FMC LA Channel 23 Data P
FMC2_LA24_N	B64_L15_N	AT19	FMC LA Channel 24 Data N
FMC2_LA24_P	B64_L15_P	AT20	FMC LA Channel 24 Data P
FMC2_LA25_N	B64_L18_N	AR17	FMC LA Channel 25 Data N
FMC2_LA25_P	B64_L18_P	AR18	FMC LA Channel 25 Data P
FMC2_LA26_N	B64_L19_N	AJ21	FMC LA Channel 26 Data N
FMC2_LA26_P	B64_L19_P	AH21	FMC LA Channel 26 Data P
FMC2_LA27_N	B64_L22_N	AK18	FMC LA Channel 27 Data N

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC2_LA27_P	B64_L22_P	AK19	FMC LA Channel 27 Data P
FMC2_LA28_N	B64_L17_N	AU18	FMC LA Channel 28 Data N
FMC2_LA28_P	B64_L17_P	AU19	FMC LA Channel 28 Data P
FMC2_LA29_N	B64_L1_N	AV22	FMC LA Channel 29 Data N
FMC2_LA29_P	B64_L1_P	AU22	FMC LA Channel 29 Data P
FMC2_LA30_N	B64_L3_N	AW21	FMC LA Channel 30 Data N
FMC2_LA30_P	B64_L3_P	AV21	FMC LA Channel 30 Data P
FMC2_LA31_N	B64_L5_N	AT21	FMC LA Channel 31 Data N
FMC2_LA31_P	B64_L5_P	AT22	FMC LA Channel 31 Data P
FMC2_LA32_N	B64_L4_N	AW19	FMC LA Channel 32 Data N
FMC2_LA32_P	B64_L4_P	AW20	FMC LA Channel 32 Data P
FMC2_LA33_N	B64_L2_N	AV20	FMC LA Channel 33 Data N
FMC2_LA33_P	B64_L2_P	AU20	FMC LA Channel 33 Data P
FMC2_SCL	B90_L2_P	F4	FMC I2C Bus Clock
FMC2_SDA	B90_L2_N	E3	FMC I2C Bus Data
FMC2_HPC_GBTCLK0_M2C_C_N	MGT224_CLK0_N	AM9	Transceiver Reference Clock 0 Input N
FMC2_HPC_GBTCLK0_M2C_C_P	MGT224_CLK0_P	AM10	Transceiver Reference Clock 0 Input P
MGT_A_CLOCK_N	MGT224_CLK1_N	AK9	Transceiver Reference Clock 1 Input N
MGT_A_CLOCK_P	MGT224_CLK1_P	AK10	Transceiver Reference Clock 1 Input P
FMC2_DP0_M2C_P	MGT224_RX3_P	AT2	Transceiver Data 0 Input P
FMC2_DP0_M2C_N	MGT224_RX3_N	AT1	Transceiver Data 0 Input N
FMC2_DP1_M2C_P	MGT224_RX2_P	AU4	Transceiver Data 1 Input P
FMC2_DP1_M2C_N	MGT224_RX2_N	AU3	Transceiver Data 1 Input N
FMC2_DP2_M2C_P	MGT224_RX0_P	AW4	Transceiver Data 2 Input P
FMC2_DP2_M2C_N	MGT224_RX0_N	AW3	Transceiver Data 2 Input N
FMC2_DP3_M2C_P	MGT224_RX1_P	AV2	Transceiver Data 3 Input P
FMC2_DP3_M2C_N	MGT224_RX1_N	AV1	Transceiver Data 3 Input N
FMC2_DP4_M2C_P	MGT225_RX1_P	AP2	Transceiver Data 4 Input P

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Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
FMC2_DP4_M2C_N	MGT225_RX1_N	AP1	Transceiver Data 4 Input N
FMC2_DP5_M2C_P	MGT225_RX3_P	AM2	Transceiver Data 5 Input P
FMC2_DP5_M2C_N	MGT225_RX3_N	AM1	Transceiver Data 5 Input N
FMC2_DP6_M2C_P	MGT225_RX2_P	AN4	Transceiver Data 6 Input P
FMC2_DP6_M2C_N	MGT225_RX2_N	AN3	Transceiver Data 6 Input N
FMC2_DP7_M2C_P	MGT225_RX0_P	AR4	Transceiver Data 7 Input P
FMC2_DP7_M2C_N	MGT225_RX0_N	AR3	Transceiver Data 7 Input N
FMC2_DP0_C2M_P	MGT224_TX3_P	AT6	Transceiver Data 0 Output P
FMC2_DP0_C2M_N	MGT224_TX3_N	AT5	Transceiver Data 0 Output N
FMC2_DP1_C2M_P	MGT224_TX2_P	AU8	Transceiver Data 1 Output P
FMC2_DP1_C2M_N	MGT224_TX2_N	AU7	Transceiver Data 1 Output N
FMC2_DP2_C2M_P	MGT224_TX0_P	AW8	Transceiver Data 2 Output P
FMC2_DP2_C2M_N	MGT224_TX0_N	AW7	Transceiver Data 2 Output N
FMC2_DP3_C2M_P	MGT224_TX1_P	AV6	Transceiver Data 3 Output P
FMC2_DP3_C2M_N	MGT224_TX1_N	AV5	Transceiver Data 3 Output N
FMC2_DP4_C2M_P	MGT225_TX1_P	AP6	Transceiver Data 4 Output P
FMC2_DP4_C2M_N	MGT225_TX1_N	AP5	Transceiver Data 4 Output N
FMC2_DP5_C2M_P	MGT225_TX3_P	AM6	Transceiver Data 5 Output P
FMC2_DP5_C2M_N	MGT225_TX3_N	AM5	Transceiver Data 5 Output N
FMC2_DP6_C2M_P	MGT225_TX2_P	AN8	Transceiver Data 6 Output P
FMC2_DP6_C2M_N	MGT225_TX2_N	AN7	Transceiver Data 6 Output N
FMC2_DP7_C2M_P	MGT225_TX0_P	AR8	Transceiver Data 7 Output P
FMC2_DP7_C2M_N	MGT225_TX0_N	AR7	Transceiver Data 7 Output N
FMC2_HPC_GBTCLK1_M2C_C_N	MGT225_CLK0_N	AJ11	Transceiver Reference Clock 0 Input N
FMC2_HPC_GBTCLK1_M2C_C_P	MGT225_CLK0_P	AJ12	Transceiver Reference Clock 0 Input P

Table 3.4.2 - FMC HPC J13 Connector Pin Assignment

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3.5 MIPI Interface

The AXKU15S carrier board has two MIPI lanex4 camera input interfaces. MIPI1 corresponds to J9 and connects to BANK69 and BANK90 of the FPGA . MIPI2 corresponds to J10 and connects to BANK71 and BANK90 of the FPGA . The connection design diagram is shown in the figure below:

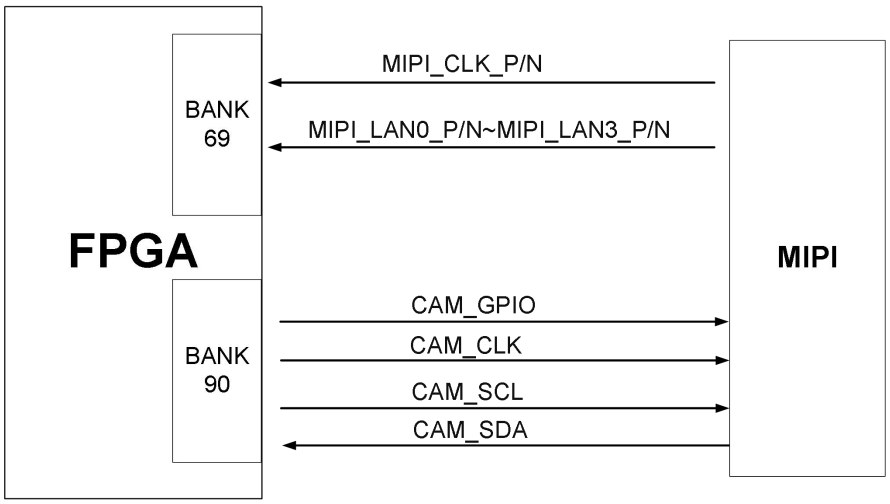


Figure 3.5.1 - MIPI1 Interface Design Schematic

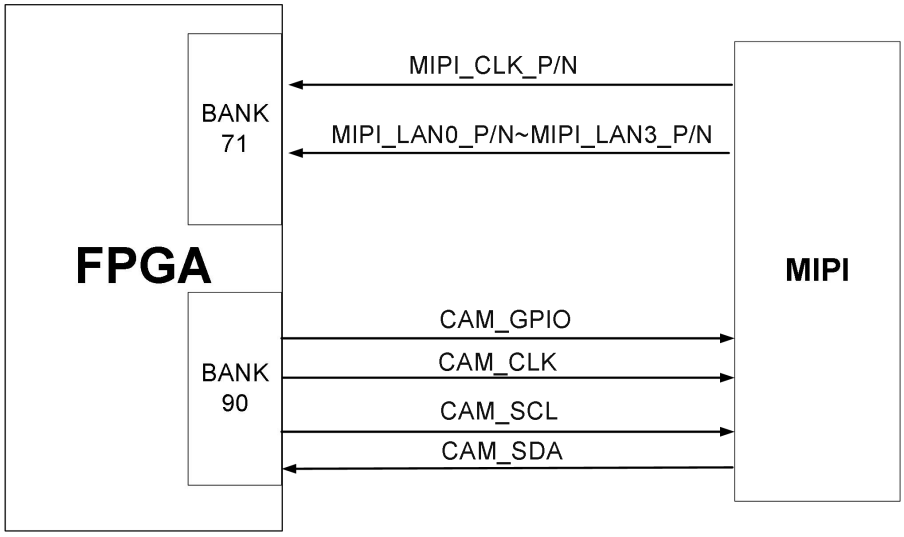


Figure 3.5.2 - MIPI2 Interface Design Schematic

MIPI 1 interface pin assignment

Signal name	FPGA pin names	FPGA pin numbers	Remark
MIPI1_CLK_P	B69_L19_P	C29	MIPI input clock positive
MIPI1_CLK_N	B69_L19_N	B29	MIPI input clock negative

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Signal name	FPGA pin names	FPGA pin numbers	Remark
MIPI1_LAN0_P	B69_L23_P	B26	MIPI input data LANE0 is positive
MIPI1_LAN0_N	B69_L23_N	A26	MIPI input data LANE0 negative
MIPI1_LAN1_P	B69_L20_P	C27	MIPI input data LANE1 is positive
MIPI1_LAN1_N	B69_L20_N	C28	MIPI input data LANE1 negative
MIPI1_LAN2_P	B69_L21_P	B31	MIPI input data LANE 2 positive
MIPI1_LAN2_N	B69_L21_N	A31	MIPI input data LANE 2 negative
MIPI1_LAN3_P	B69_L22_P	B27	MIPI input data LANE 3 positive
MIPI1_LAN3_N	B69_L22_N	A27	MIPI input data LANE 3 negative
MIPI1_CLK	B90_L8_P	C5	Camera clock input
MIPI1_GPIO	B90_L8_N	C4	Camera GPIO control
MIPI1_I2C_SCL	B90_L3_P	F3	Camera I2C clock
MIPI1_I2C_SDA	B90_L3_N	F2	I2C data from the camera

Table 3.5.1 - MIPI 1 Interface Pin Assignment

MIPI 2 interface pin assignment

Signal name	FPGA pin names	FPGA pin numbers	Remark
MIPI2_CLK_P	B71_L1_P	M16	MIPI input clock positive
MIPI2_CLK_N	B71_L1_N	M15	MIPI input clock negative
MIPI2_LAN0_P	B71_L3_P	L18	MIPI input data LANE0 is positive
MIPI2_LAN0_N	B71_L3_N	K18	MIPI input data LANE0 negative
MIPI2_LAN1_P	B71_L5_P	K16	MIPI input data LANE1 is positive
MIPI2_LAN1_N	B71_L5_N	J16	MIPI input data LANE1 negative
MIPI2_LAN2_P	B71_L2_P	L19	MIPI input data LANE 2 positive
MIPI2_LAN2_N	B71_L2_N	K19	MIPI input data LANE 2 negative
MIPI2_LAN3_P	B71_L4_P	L17	MIPI input data LANE 3 positive
MIPI2_LAN3_N	B71_L4_N	L16	MIPI input data LANE 3 negative
MIPI2_CLK	B90_L7_P	D3	Camera clock input
MIPI2_GPIO	B90_L7_N	C3	Camera GPIO control

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Signal name	FPGA pin names	FPGA pin numbers	Remark
MIPI2_I2C_SCL	B90_L4_P	F1	Camera I2C clock
MIPI2_I2C_SDA	B90_L4_N	E1	I2C data from the camera

Table 3.5.2 - MIPI 2 Interface Pin Assignment

3.6 USB to Serial Port

The AXKU15S carrier board is equipped with a UART-to-USB interface for system debugging. The converter chip is the Silicon Labs CP2102N USB- UART chip , and the USB interface is a MINI USB interface. It can be connected to a PC 's USB port using a single USB cable for independent power supply and serial data communication to the SoM. A schematic diagram of the USB UART circuit design is shown below :

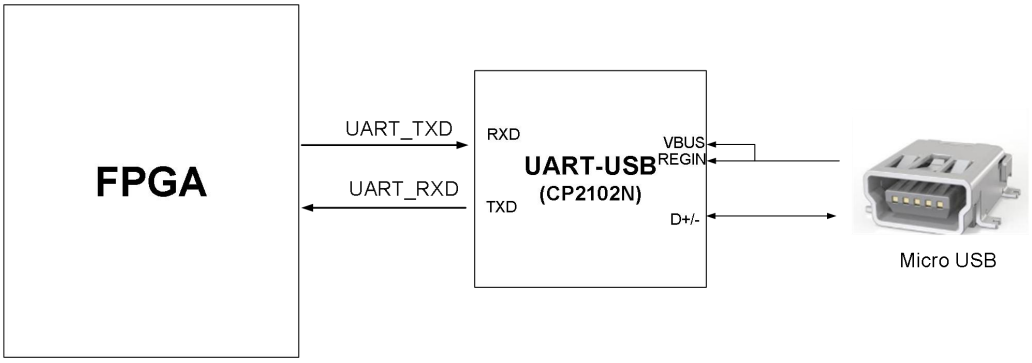


Figure 3.6.1 - Schematic diagram of USB to serial port adapter

FPGA pin assignment for USB to serial port conversion:

Signal name	FPGA pin names	pin number	Remark
UART_RXD	B90_L6_N	D1	UART data input
UART_TXD	B90_L6_P	D2	UART data output

Table 3.6.1 - USB to Serial Port Pin Assignment

3.7 SD Card Slot

The AXKU15S carrier board includes a MicroSD card interface, providing users with access to SD card storage for user data files. The SDIO signal is connected to the FPGA's I/O signals , supporting both SPI and SD modes, and uses a MicroSD card. The schematic diagram of the FPGA and SD card connector is shown below.

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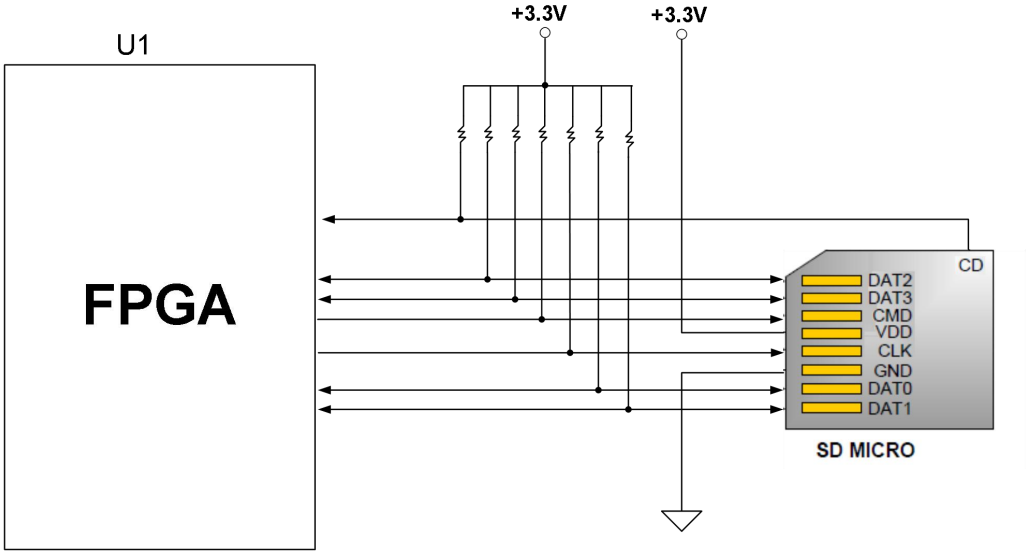


Figure 3.7.1 - SD Card Slot Schematic Diagram

SD card slot pin assignment

Signal name	FPGA pin names	FPGA pin numbers	Remark
SD_CD	IO_L11N_AD1N_90	A3	SD chip select signal
SD_CLK	IO_L8P_HDGC_91	C10	SD clock signal
SD_CMD	IO_L8N_HDGC_91	C9	SD command signals
SD_D0	IO_L12N_AD0N_90	A6	SD Data0
SD_D1	IO_L12P_AD0P_90	B6	SD Data1
SD_D2	IO_L7N_HDGC_91	C7	SD Data2
SD_D3	IO_L7P_HDGC_91	C8	SD Data3

Table 3.7.1 - SD Card Slot Pin Assignment

3.8 SATA Interfaces

The development board is equipped with t'wo SATA interfaces, and the differential signals of the SATA interfaces are connected to the GTY BANK 131 .

The SATA reference clock of 150 MHz is provided by the programmable clock chip Si5332BD11025-4. The schematic diagram of the SATA interface design is shown below:

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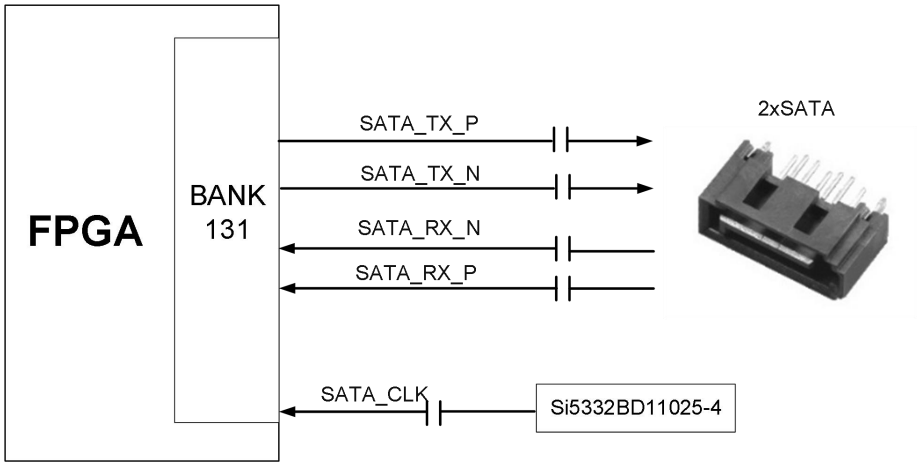


Figure 3.8.1 - SATA Interface Design Diagram

The SATA interface FPGA pin assignments are as follows:

Signal Name	FPGA Pin Name	FPGA Pin Number	Remarks
SATA1_RX_N	MGTYRXN0_131	M37	SATA1 Data Receive Negative
SATA1_RX_P	MGTYRXP0_131	M36	SATA1 Data Receive Positive
SATA2_RX_N	MGTYRXN1_131	L39	SATA2 Data Receive Negative
SATA2_RX_P	MGTYRXP1_131	L38	SATA2 Data Receive Positive
SATA1_TX_N	MGTYTXN0_131	J34	SATA1 Data Transmit Negative
SATA1_TX_P	MGTYTXP0_131	J33	SATA1 Data Transmit Positive
SATA2_TX_N	MGTYTXN1_131	G34	SATA2 Data Transmit Negative
SATA2_TX_P	MGTYTXP1_131	G33	SATA2 Data Transmit Positive
SATACLK_N	MGTREFCLK0N_131	T28	SATA Reference Clock Negative
SATACLK_P	MGTREFCLK0P_131	T27	SATA Reference Clock Positive

Table 3.8.1 - SATA Pin Assignment

3.9 Button and LED

The AXKU15S carrier board has 7 LEDs , 1 power indicator, 2 serial communication indicator lights, and 4 user LEDs. The power indicator light illuminates when the development board is powered on. The 4 LEDs are connected to the FPGA's I/O pins, allowing users to control their on/off state via a program. When the I/O voltage connected to a user LED is high , the LED is lit ; when the I/O voltage is low , the LED is off. Additionally, the board has 4 user buttons. The default button signal is high; when a button is pressed, the button signal is low. A hardware connection diagram of the user LEDs and buttons is shown in the figure.

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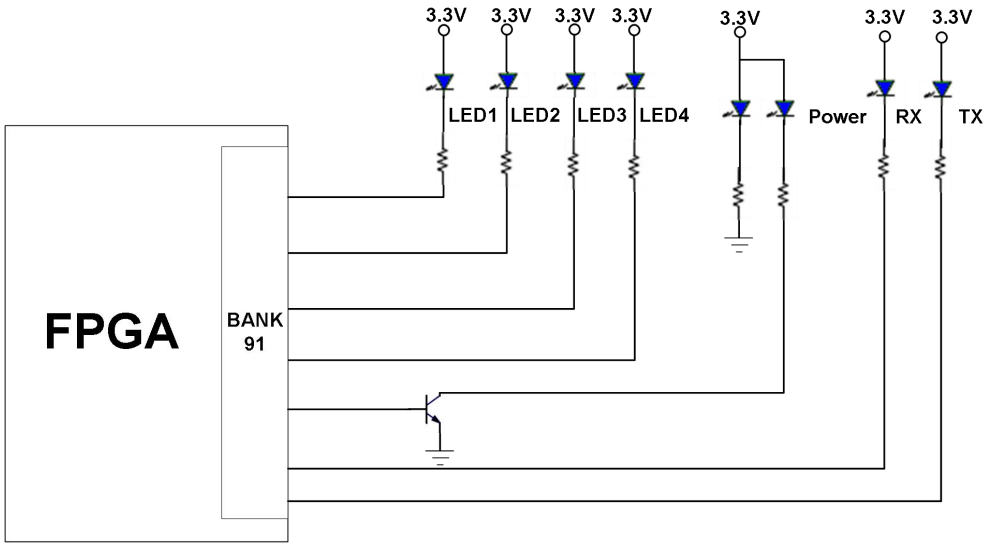


Figure 3.9.1 - Schematic diagram of hardware connection for user LED lights and buttons

Pin assignment for user LEDs and buttons

Signal name	FPGA pin names	Pin number	Remark
KEY1	B91_L9_P	A8	User button 1
KEY2	B91_L9_N	B9	User button 2
KEY3	B91_L10_P	A7	User button 3
KEY4	B91_L10_N	B7	User button 4
LED1	B91_L5_P	D8	User LED1 light
LED2	B91_L5_N	D7	User LED2 light
LED3	B91_L6_P	D11	User LED 3 light
LED4	B91_L6_N	D10	User LED 4 light

Table 3.9.1 - LED and Button Pin Assignments

3.10 EEPROM

The AXKU15S development board features an onboard EEPROM, model 24LC04, with a capacity of 4Kbit (2*256*8bit), consisting of two 256-byte blocks, communicating via the I2C bus. The onboard EEPROM is used to learn the I2C bus communication method.The EEPROM's I2C signals are connected to the FPGA's BANK 90 IO port. The following diagram shows the EEPROM's design schematic .

.

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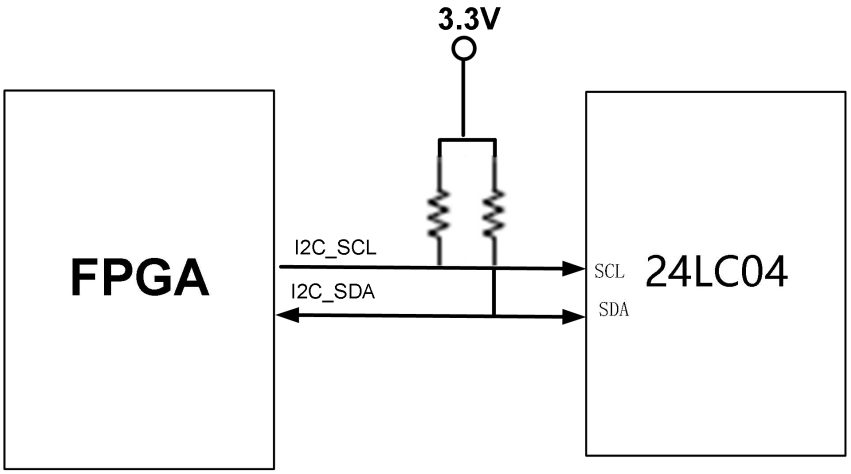


Figure 3.10.1 - EEPROM Schematic Diagram

EEPROM pin assignment:

Pin Name	FPGA pin names	FPGA pins
EEPROM_RTC_I2C_SCL	IO_L9N_AD3N_90	B2
EEPROM_RTC_I2C_SDA	IO_L9P_AD3P_90	C2

Table 3.10.1 - EEPROM Pin Assignment

3.11 Temperature Sensor

The AXKU15S development board is equipped with a high-precision, low-power digital temperature sensor chip, the ON Semiconductor LM75 A. The LM75 A chip has a temperature accuracy of 0.125 degrees Celsius. The sensor and FPGA share a direct I2C digital interface; the FPGA reads the temperature near the development board via the I2C interface. The following diagram shows the design schematic of the LM75 A sensor chip.

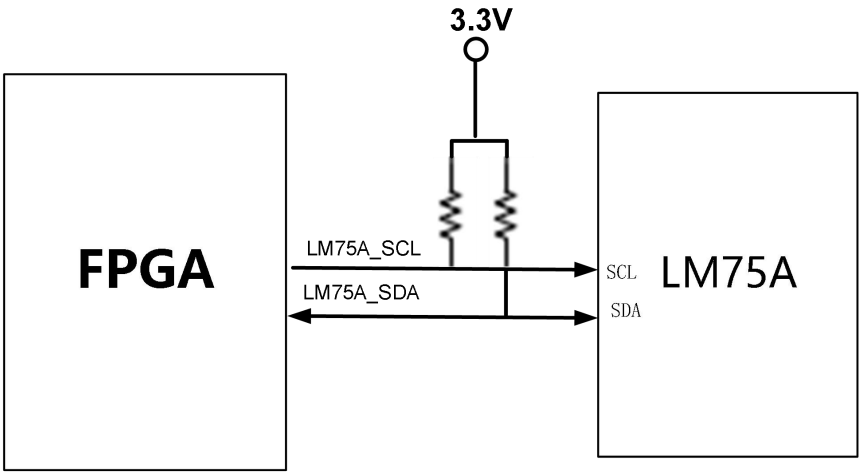


Figure 3.11.1 - Partial schematic diagram of the LM75A sensor

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LM75 A sensor pin assignment:

Pin Name	FPGA pin names	FPGA pin numbers
LM75A_SCL	IO_L10P_AD2P_90	B5
LM75A_S DA	IO_L10N_AD2N_90	B4

Table 3.11.1 - LM75 A Sensor Pin Assignment

3.12 Fiber Optic Interface

The carrier board has two QSFP28 fiber optic interfaces. Users can purchase QSFP optical modules and insert them into these four fiber optic interfaces for fiber optic data communication. The two fiber optic interfaces are respectively connected to the four RX/TX channels of the GTY transceiver on the FPGA 's BANK127-128. The FPGA and fiber optic design schematic is shown in the following figure:

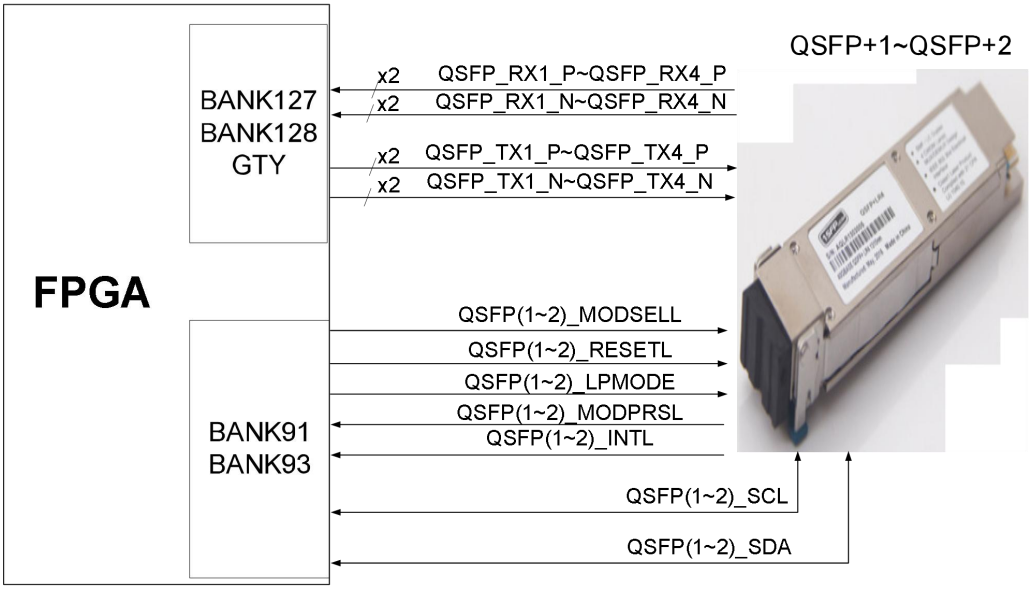


Figure 3.12.1 - Schematic diagram of fiber optic design

The pin assignments for the two fiber optic interfaces are as follows:

Pin Name	FPGA Pin Name	FPGA Pin Number	Remarks
QSFP1_RX1_N	MGTYRXN0_127	AH37	QSFP Module 1 Lane 1 Receive Negative
QSFP1_RX1_P	MGTYRXP0_127	AH36	QSFP Module 1 Lane 1 Receive Positive
QSFP1_RX2_N	MGTYRXN1_127	AG39	QSFP Module 1 Lane 2 Receive Negative
QSFP1_RX2_P	MGTYRXP1_127	AG38	QSFP Module 1 Lane 2 Receive Positive

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Pin Name	FPGA Pin Name	FPGA Pin Number	Remarks
QSFP1_RX3_N	MGTYRXN2_127	AF37	QSFP Module 1 Lane 3 Receive Negative
QSFP1_RX3_P	MGTYRXP2_127	AF36	QSFP Module 1 Lane 3 Receive Positive
QSFP1_RX4_N	MGTYRXN3_127	AE39	QSFP Module 1 Lane 4 Receive Negative
QSFP1_RX4_P	MGTYRXP3_127	AE38	QSFP Module 1 Lane 4 Receive Positive
QSFP1_TX1_N	MGTYTXN0_127	AF32	QSFP Module 1 Lane 1 Transmit Negative
QSFP1_TX1_P	MGTYTXP0_127	AF31	QSFP Module 1 Lane 1 Transmit Positive
QSFP1_TX2_N	MGTYTXN1_127	AE34	QSFP Module 1 Lane 2 Transmit Negative
QSFP1_TX2_P	MGTYTXP1_127	AE33	QSFP Module 1 Lane 2 Transmit Positive
QSFP1_TX3_N	MGTYTXN2_127	AD32	QSFP Module 1 Lane 3 Transmit Negative
QSFP1_TX3_P	MGTYTXP2_127	AD31	QSFP Module 1 Lane 3 Transmit Positive
QSFP1_TX4_N	MGTYTXN3_127	AC34	QSFP Module 1 Lane 4 Transmit Negative
QSFP1_TX4_P	MGTYTXP3_127	AC33	QSFP Module 1 Lane 4 Transmit Positive
QSFP1_SCL	IO_L1P_AD15P_91	F6	I2C Clock for QSFP Module 1
QSFP1_SDA	IO_L2P_AD14P_91	F8	I2C Data for QSFP Module 1
QSFP1_INTL	IO_L10P_AD2P_93	L13	Interrupt Signal of QSFP Module 1
QSFP1_LPMODE	IO_L2N_AD14N_91	F7	Low Power Mode Select Signal of QSFP 1
QSFP1_MODPRSL	IO_L10N_AD2N_93	K13	Module Present Indicator of QSFP 1
QSFP1_MODSELL	IO_L9N_AD3N_93	M10	Module Select Signal of QSFP Module 1
QSFP1_RESETL	IO_L9P_AD3P_93	N10	Reset Signal of QSFP Module 1
QSFP2_RX1_N	MGTYRXN0_128	AD37	QSFP Module 2 Lane 1 Receive Negative
QSFP2_RX1_P	MGTYRXP0_128	AD36	QSFP Module 2 Lane 1 Receive Positive
QSFP2_RX2_N	MGTYRXN1_128	AC39	QSFP Module 2 Lane 2 Receive Negative
QSFP2_RX2_P	MGTYRXP1_128	AC38	QSFP Module 2 Lane 2 Receive Positive
QSFP2_RX3_N	MGTYRXN2_128	AB37	QSFP Module 2 Lane 3 Receive Negative
QSFP2_RX3_P	MGTYRXP2_128	AB36	QSFP Module 2 Lane 3 Receive Positive
QSFP2_RX4_N	MGTYRXN3_128	AA39	QSFP Module 2 Lane 4 Receive Negative
QSFP2_RX4_P	MGTYRXP3_128	AA38	QSFP Module 2 Lane 4 Receive Positive
QSFP2_TX1_N	MGTYTXN0_128	AB32	QSFP Module 2 Lane 1 Transmit Negative

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Pin Name	FPGA Pin Name	FPGA Pin Number	Remarks
QSFP2_TX1_P	MGTYTXP0_128	AB31	QSFP Module 2 Lane 1 Transmit Positive
QSFP2_TX2_N	MGTYTXN1_128	AA34	QSFP Module 2 Lane 2 Transmit Negative
QSFP2_TX2_P	MGTYTXP1_128	AA33	QSFP Module 2 Lane 2 Transmit Positive
QSFP2_TX3_N	MGTYTXN2_128	Y32	QSFP Module 2 Lane 3 Transmit Negative
QSFP2_TX3_P	MGTYTXP2_128	Y31	QSFP Module 2 Lane 3 Transmit Positive
QSFP2_TX4_N	MGTYTXN3_128	W34	QSFP Module 2 Lane 4 Transmit Negative
QSFP2_TX4_P	MGTYTXP3_128	W33	QSFP Module 2 Lane 4 Transmit Positive
QSFP2_SCL	IO_L5N_HDGC_AD7N_93	N14	I2C Clock for QSFP Module 2
QSFP2_SDA	IO_L5P_HDGC_AD7P_93	N15	I2C Data for QSFP Module 2
QSFP2_INTL	IO_L1P_AD11P_93	R15	Interrupt Signal of QSFP Module 2
QSFP2_LPMODE	IO_L6N_HDGC_AD6N_93	N12	Low Power Mode Select Signal of QSFP 2
QSFP2_MODPRSL	IO_L1N_AD11N_93	P15	Module Present Indicator of QSFP 2
QSFP2_MODSELL	IO_L2N_AD10N_93	R13	Module Select Signal of QSFP Module 2
QSFP2_RESETL	IO_L2P_AD10P_93	R14	Reset Signal of QSFP Module 2

Table 3.12.1 - Fiber Optic Interface Pin Assignment

3.13 JTAG

A 10-pin JTAG interface is provided on the AXKU15S carrier board for downloading FPGA programs or burning programs to FLASH. To prevent damage to the FPGA chip from hot-plugging, a protection diode is added to the JTAG signal to ensure that the signal voltage is within the acceptable range for the FPGA, thus avoiding chip damage. The FPGA and JTAG pin assignments are shown in the table below :

Pin Name	FPGA pin names	FPGA pin numbers	Remark
FPGA_TDO	TDO_0	AG27	TDO Output
FPGA_TCK	TCK_0	AG23	TCK Clock
FPGA_TDI	TDI_0	AG24	TDI Input
FPGA_TMS	TMS_0	AD22	TMS Mode Select

Table 3.13.1 - JTAG Interface Pin Assignment

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3.14 Clock Configuration

The AXKU15S carrier board has two differential clock sources, G2 and G3, operating at 156.25 MHz to provide reference clocks for the FPGA's high-speed transceivers. Additionally, the reference clocks for BANK 127 and BANK 128 can be sourced either from the Si5332BD 11025-4 chip or from independent crystal oscillators. The clock circuit schematic is shown in Figure 3.14.1 below:

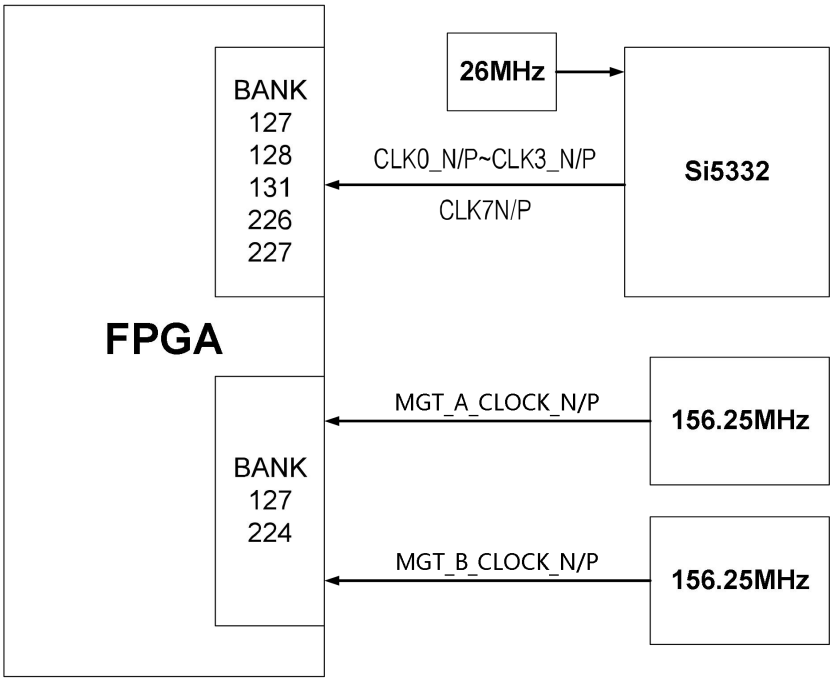


Figure 3.14.1 - Power interface section in the schematic diagram

The FPGA and clock pin assignments are shown in the table below :

Pin Name	FPGA pin names	FPGA pin numbers	Remark
MGT_B_CLOCK_P	MGTREFCLK1P_127	AC29	High-speed transceiver reference clock positive B
MGT_A_CLOCK_N	MGTREFCLK1N_224	AK9	High-speed transceiver reference clock negative A
MGT_A_CLOCK_P	MGTREFCLK1P_224	AK10	High-speed transceiver reference clock positive A
MGT_B_CLOCK_N	MGTREFCLK1N_127	AC30	High-speed transceiver reference clock negative B
CLK0_N	MGTREFCLK0N_127	AE30	Clock 0 input N
CLK0_P	MGTREFCLK0P_127	AE29	Clock 0 input P
CLK1_N	MGTREFCLK0N_128	AB28	Clock 1 input N
CLK1_P	MGTREFCLK0P_128	AB27	Clock 1 input P
CLK2_N	MGTREFCLK1N_227	AD9	Clock 2 input N

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Pin Name	FPGA pin names	FPGA pin numbers	Remark
CLK2_P	MGTREFCLK1P_227	AD10	Clock 2 input P
CLK3_N	MGTREFCLK1N_128	AA30	Clock 3 input N
CLK3_P	MGTREFCLK1P_128	AA29	Clock 3 input P
CLK7_N	MGTREFCLK1N_226	AF9	Clock 7 input N
CLK7_P	MGTREFCLK1P_226	AF10	Clock 7 input P

Table 3.14.1 - Clock Signal Pin Assignment

3.15 Power Supply

The development board's power input voltage is DC12V, and it can be powered via a PCIe slot or an external +12V power supply. When using an external power supply, please use the power supply provided with the development board; do not use other power supplies to avoid damaging the board. The four DC/DC power chips SGM61163 output +5V, FMC1_VADJ, FMC2_VADJ, and 3.3V respectively; the ETA1471 outputs the voltage required by the FPGABANK . Simultaneously, the +3.3V output supplies the voltage required by each FPGABANK in the multi-channel LDO output JTAG . The SoM BANK69-71 is powered by a DC-DC chip by default, while BANK90-94 is connected to 3.3V by default. Users can select the LDO chip power supply using resistors. The power supply design diagram is shown below:

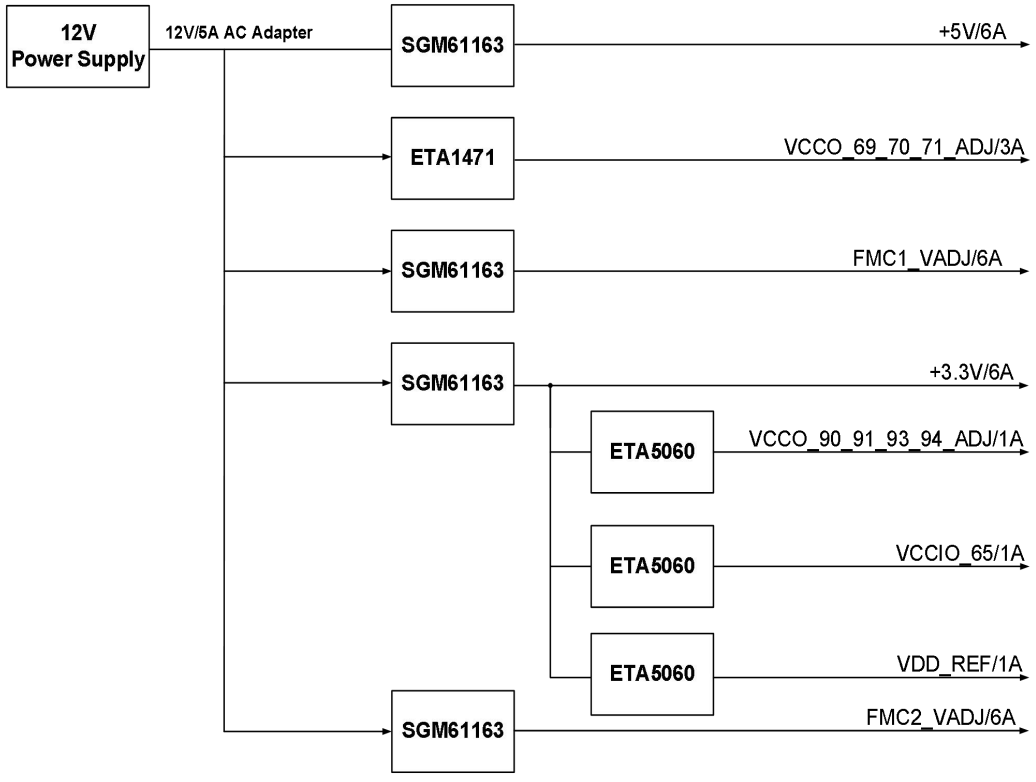


Figure 3.15.1 - Power interface section in the schematic diagram

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The functions of each power distribution unit are shown in the table below:

power supply	Function
+5.0V	Expansion module power supply
FMC1_VADJ	FMC1 adjusts voltage
FMC2_VADJ	FMC2 adjusts voltage
+3.3V	External power supply for carrier board
VDD_REF	JTAG power supply
VCCIO_65	FPGA BANK voltage
VCCIO_90_91_93_94_ADJ@1A	FPGA BANK voltage
VCCIO_69_70_71_ADJ@1A	FPGA BANK voltage

Table 3.15.1 - Power Function Allocation

3.16 Structural Dimensions Drawing

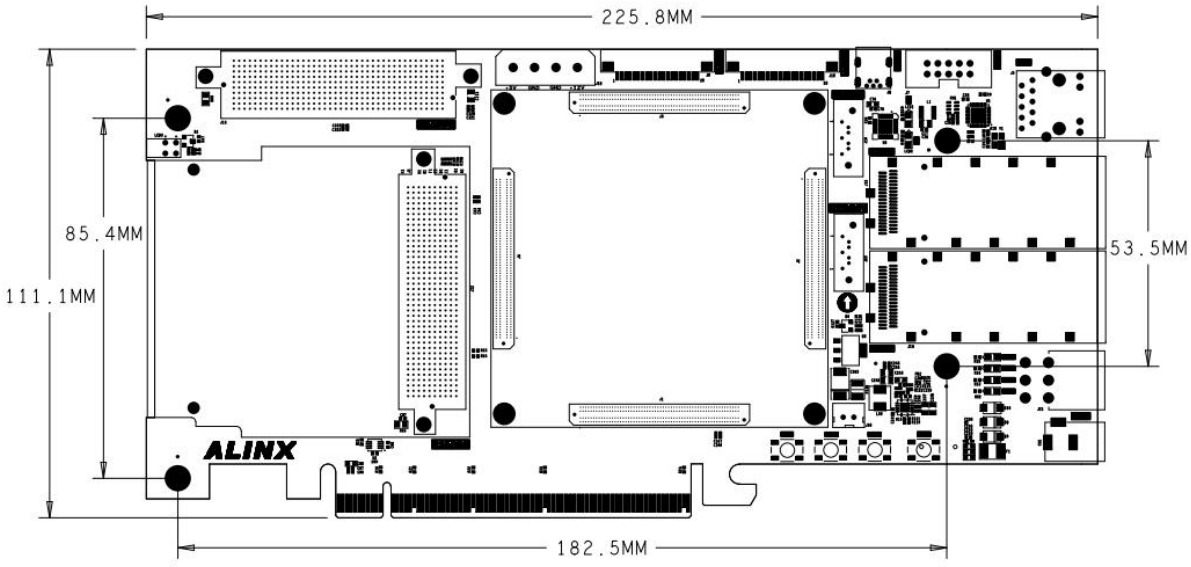


Figure 3.16.1 - Top View of the Development Board

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